Component and Measurement Advances Ensure 16-Bit DAC Settling Time

The art of timely accuracy

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Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas are beginning to utilize 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have seen increasing use. New components (see Components for 16-Bit Digital-to-Analog Conversion, page 2) have made 16-bit DACs a practical design alternative[1]. These ICs provide 16-bit performance at reasonable cost compared to previous modular and hybrid technologies. The DC and AC specifications of the monolithic DAC's approach or equal previous converters at significantly lower cost.

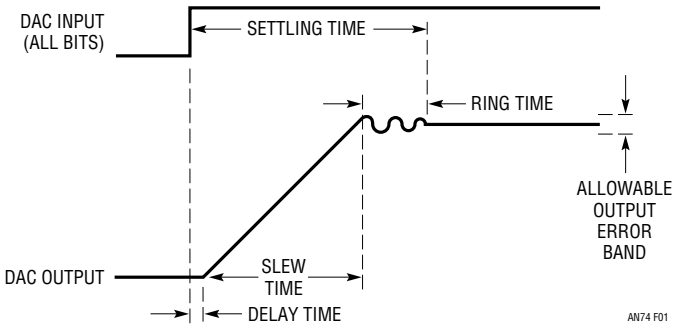

Figure 1. DAC Settling Time Components Include Delay, Slew and Ring Times. Fast Amplifiers Reduce Slew Time, Although Longer Ring Time Usually Results. Delay Time is Normally a Small Term

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of the DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution. DAC settling time is the elapsed time from input code application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval there is no output movement. During *slew time* the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs which degrade DC error terms.[2]

Measuring anything at any speed to 16 bits (≈0.0015%) is hard. Dynamic measurement to 16-bit resolution is particularly challenging. Reliable 16-bit settling time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.

Note 1. See Appendix A, "A History of High Accuracy Digital-to-Analog Conversion".

Note 2. This issue is treated in detail in latter portions of the text. Also see Appendix D "Practical Considerations for DAC-Amplifier Compensation.

COMPONENTS FOR 16-BIT D/A CONVERSION

Components suitable for 16-bit D/A conversion are members of an elite class. 16 binary bits is one part in 65,536—just 0.0015% or 15 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The digital-to-analog converters listed in the chart all use Si-Chrome thin-film resistors for high stability and linearity over temperature. Gain drift is typically 1ppm/°C or about 2LSBs over 0°C to 70°C. The amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 16-bit DAC driven settling times of 1.7µs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05%

Short Form Descriptions of Components Suitable for 16-Bit Digital-to-Analog Conversion

COMPONENT TYPE	ERROR CONTRIBUTION OVER 0°C TO 70°C	COMMENTS
LTC®1597 DAC	≈2LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Output
LTC1595 DAC	≈2LSB Gain Drift 1LSB Linearity	Serial Input 8-PIn Package Current Output
LTC1650 DAC	≈3.5LSB Gain Drift 6LSB Offset 4LSB Linearity	Complete Voltage Output DAC
LT®1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468 Amplifier	<2LSB	1.7µs Settling to 16 Bits Fastest Available
LM199A Reference-6.95V	≈1LSB	Lowest Drift Reference in This Group
LT1021 Reference-10V	≈4LSB	Good General Purpose Choice
LT1027 Reference-5V	≈4LSB	Good General Purpose Choice
LT1236 Reference-10V	≈10LSB	Trimmed to 0.05% Absolute Accuracy
LT1461 Reference-4.096V	≈10LSB	Recommended for LTC1650 DACs (see Above)

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the "false sum node" technique. The resistors and DAC-amplifier form a bridge type network. Assuming ideal resistors, the amplifier output will step to V_{IN} when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but

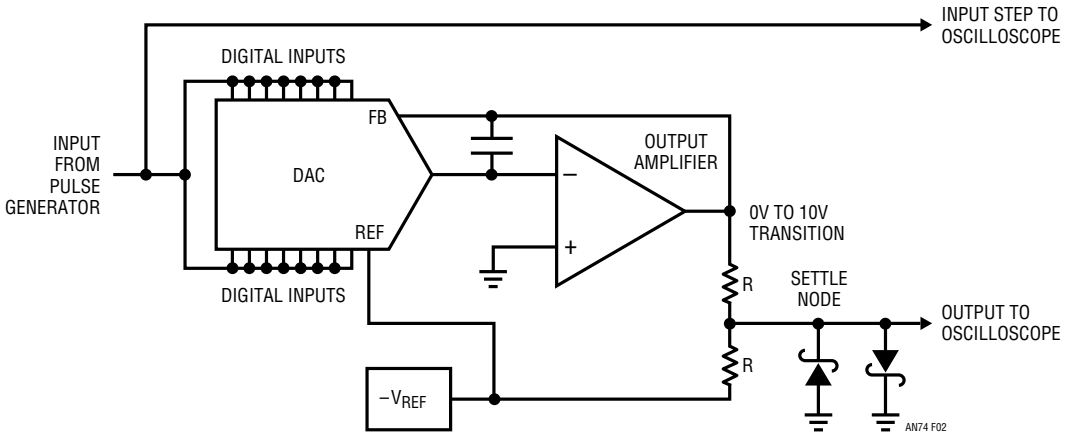

Figure 2. Popular Summing Scheme for DAC Settling Time Measurement Provides Misleading Results. 16-Bit Measurement Causes >200× Oscilloscope Overdrive. Displayed Information is Meaningless

its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active 1× FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question.[3]

At 10-bit resolution (10mV at the DAC output—5mV at the oscilloscope), the oscilloscope typically undergoes a 2× overdrive at 50mV/DIV, and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 16 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 16-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope.[4] Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling 'scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring 16-bit DAC settling time.

Practical DAC Settling Time Measurement

Figure 3 is a conceptual diagram of a 16-bit DAC settling-time-measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Note 3: For a discussion of oscilloscope overdrive considerations, see Appendix B, "Evaluating Oscilloscope Overdrive Performance".

Note 4: Classical sampling oscilloscopes should not be confused with modern era digital sampling 'scopes that have overdrive restrictions. See Appendix B, "Evaluating Oscilloscope Overload Performance" for comparisons of various type 'scopes with respect to overdrive. For detailed discussion of classical sampling 'scope operation see references 14 through 17 and 20 through 22. Reference 15 is noteworthy; it is the most clearly written, concise explanation of classical sampling instruments the author is aware of. A 12 page jewel.

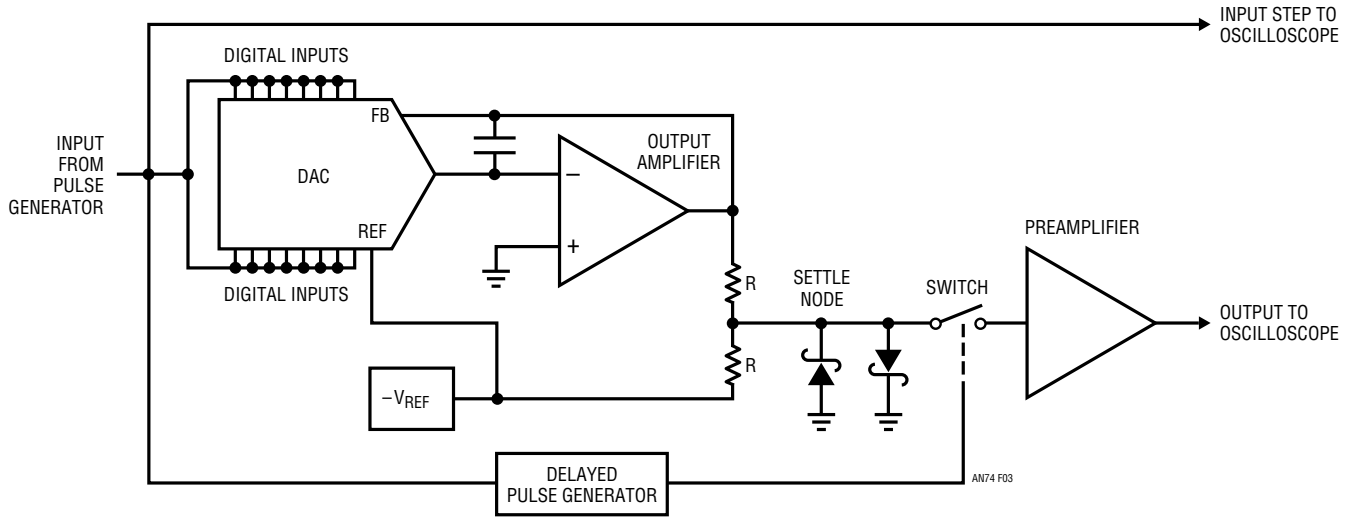

Figure 3. Conceptual Arrangement Eliminates Oscilloscope Overdrive. Delayed Pulse Generator Controls Switch, Preventing Oscilloscope from Monitoring Settle Node Until Settling is Nearly Complete

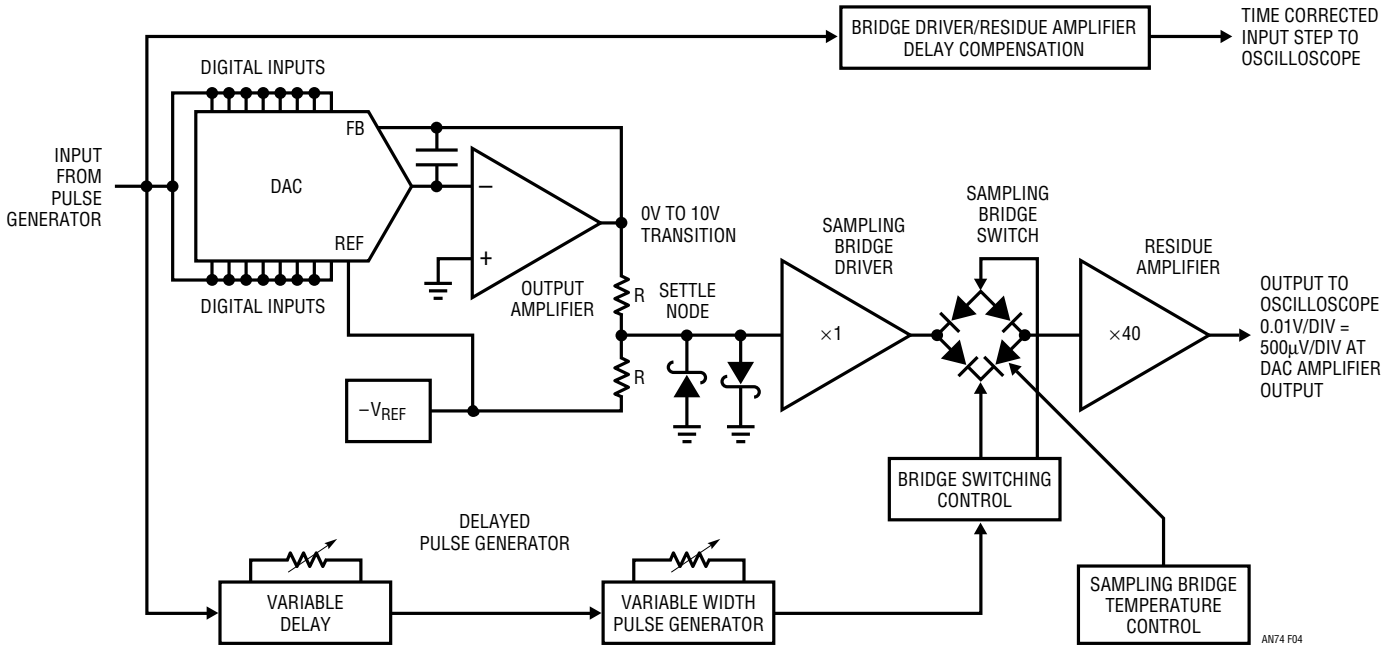

Figure 4. Block Diagram of DAC Settling Time Measurement Scheme. Diode Bridge Switch Minimizes Switching Feedthrough, Preventing Residue Amplifier-Oscilloscope Overdrive. Temperature Control Maintains 10µV Switch Offset Baseline. Input Step Time Reference is Compensated for ×1 and ×40 Amplifier Delays

Figure 4 is a more complete representation of the DAC settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling-time-measurement path. The most striking new aspect of the diagram is the diode bridge switch. Borrowed from classical sampling oscilloscope circuitry, it is the key to the measurement. The diode bridge's inherent balance eliminates charge injection based errors in the output. It is far superior to other electronic switches in this

characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switches purpose.

The diode bridge's balance, combined with matched, low capacitance monolithic diodes and complementary high speed switching, yields a cleanly switched output. The monolithic diode bridge is also temperature controlled, providing a bridge offset error below 10μV, stabilizing the measurement baseline. The temperature control is implemented using uncommitted diodes in the monolithic array as heater and sensor.

Figure 5 details considerations for the diode bridge switch. The bridge diodes tend to cancel each other's temperature coefficient—unstabilized bridge drift is about 100μV/°C and the temperature control reduces residual drift to a few microvolts/°C.

Bridge temperature control is achieved by using one diode as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7V$), serves as the heater. The control amplifier, comparing the sensor diode to a voltage at it's negative terminal, drives the heater diode to temperature stabilize the array.

DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

Detailed Settling Time Circuitry

Figure 6 is a detailed schematic of 16-bit DAC settling-time-measurement circuitry. The input pulse switches all DAC bits simultaneously and is also routed to the oscilloscope via a delay-compensation network. The delay network, composed of CMOS inverters and an adjustable RC network, compensates the oscilloscope's input step signal for the 12ns delay through the circuit's measurement path.[5] The DAC amplifier's output is compared against the LT1236-10V reference via the precision 3k summing resistor ratio set. The LT1236 also furnishes the DAC reference, making the measurement ratiometric. The clamped settle node is unloaded by A1, which drives the sampling bridge. Note the additional clamp diodes at A1's output. These diodes prevent any possibility of abnormal A1 outputs (due to lost supply or supply sequencing

Note 5: See Appendix C, "Measuring and Compensating Residue Amplifier Delay."

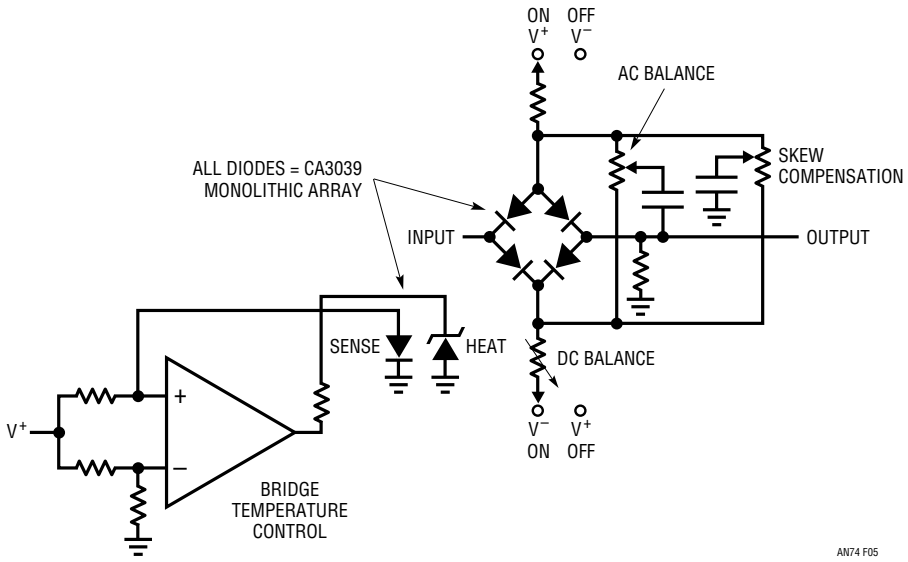

Figure 5. Diode Bridge Switch Trims Include AC and DC Balance and Switch Drive Timing Skew. Remaining Diodes in Monolithic Array are Used for Temperature Control

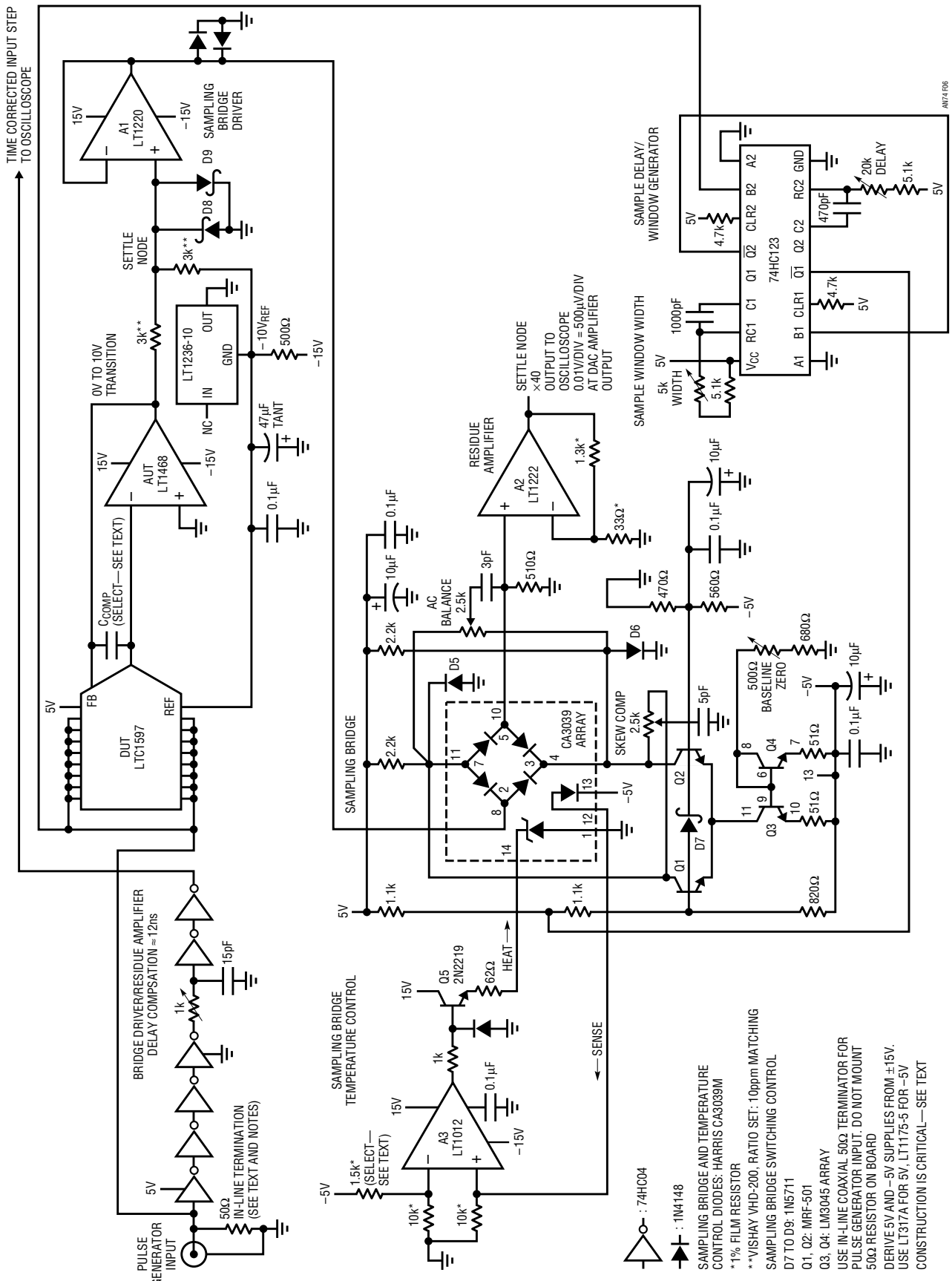

Figure 6. Detailed Schematic of DAC Settling Time Measurement Circuit Closely Follows Block Diagram. Optimum Performance Requires Attention to Layout

anomalies) from damaging the diode array.[6] A3 and associated components temperature control the sampling diode bridge by comparing a diodes's forward drop to a stable potential derived from the –5V regulator. Another diode, operated in the reverse direction ($V_Z \approx 7V$) serves as a chip heater. The pin connections shown on the schematic have been selected to provide best temperature control performance.

The input pulse triggers the 74HC123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.[7]

A2 monitors the bridge output, provides gain and drives the oscilloscope. Figure 7 shows circuit waveforms. Trace A is the input pulse, trace B the DAC amplifier output, trace C the sample gate and trace D the residue amplifier output. When the sample gate goes low, the bridge switches cleanly, and the last 1.5mV of slew are easily observed. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off, with only 600µV of feedthrough. The 100µV peak before bridge switching (at ≈3.5 vertical divisions) is feedthrough from A1's output, but it is similarly well controlled. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

The circuit requires trimming to achieve this level of performance. The bridge temperature control point is set by grounding Q5's base prior to applying power. Next, apply power and measure A3's positive input with respect to the –5V rail. Select the indicated resistor (1.5k nominal) for a voltage at A3's negative input (again, with respect to –5V) that is 57mV below the positive input's value. Unground Q5's base and the circuit will control the sampling bridge to about 55°C:

$$25°C \text{ room} + \frac{57mV}{1.9mV/°C \text{ diode drop}} = 30°C \text{ rise} = 55°C$$

The DC and AC bridge trims are made once the temperature control is functional. Making these adjustments requires disabling the DAC and amplifier (disconnect the input pulse from the DAC and set all DAC inputs low) and shorting the settle node directly to the ground plane. Figure 8 shows typical results before trimming. Trace A is the input pulse, trace B the sample gate and trace C the residue amplifier output. With the DAC-amplifier disabled

Note 6: This can and did happen. The author was unfit for human companionship upon discovering this mishap. Replacing the sampling bridge was a lengthy and highly emotionally charged task. To see why, refer to Appendix G, "Breadboarding, Layout and Connection Techniques."

Note 7: The bridge switching scheme was developed at LTC by George Feliz.

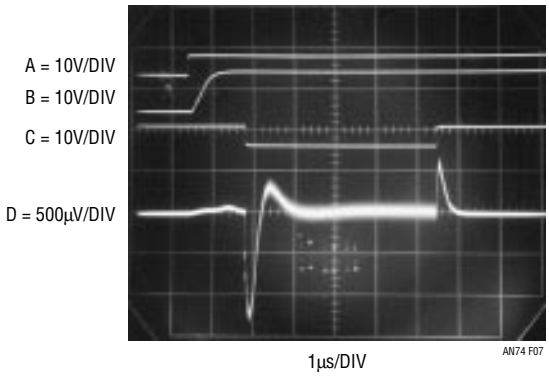

Figure 7. Settling Time Circuit Waveforms Include Time Corrected Input Pulse (Trace A), DAC Amplifier Output (Trace B), Sample Gate (Trace C) and Settling Time Output (Trace D). Sample Gate Window's Delay and Width are Variable

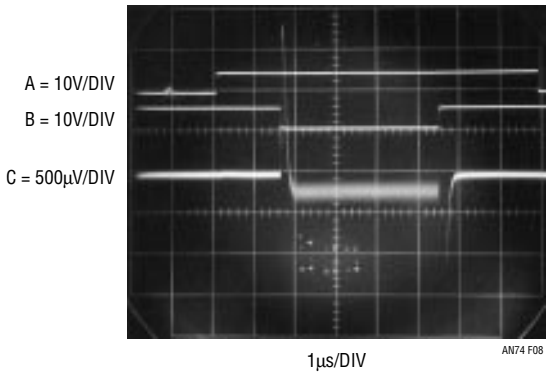

Figure 8. Settling Time Circuit's Output (Trace C) with Unadjusted Sampling Bridge AC and DC Trims. DAC is Disabled and Settle Node Grounded for This Test. Excessive Switch Drive Feedthrough and Baseline Offset are Present. Traces A and B are Input Pulse and Sample Window, Respectively

and the settle node grounded, the residue amplifier output should (theoretically) always be zero. The photo shows this is not the case for an untrimmed bridge. AC and DC errors are present. The sample gate's transitions cause large, off-screen residue amplifier swings (note residue amplifier's response to the sample gate's turn-off at the ≈8.5 vertical division). Additionally, the residue amplifier output shows significant DC offset error during the sampling interval. Adjusting the AC balance and skew compensation minimizes the switching induced transients. The DC offset is adjusted out with the baseline zero trim. Figure 9 shows the results after making these adjustments. All switching related activity is now well on-screen and offset error reduced to unreadable levels. Once this level of performance has been achieved, the circuit is ready for use.[8] Unground the settle node and restore the input pulse connection to the DAC.

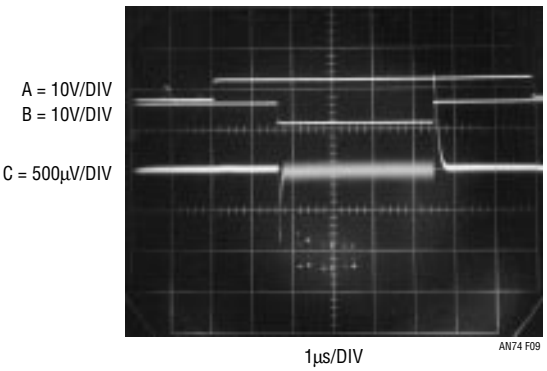

Figure 9. Settling Time Circuit's Output (Trace C) with Sampling Bridge Trimmed. As in Figure 8, DAC is Disabled and Settle Node Grounded for This Test. Switch Drive Feedthrough and Baseline Offset are Minimized. Traces A and B are Input Pulse and Sampling Gate, Respectively

Using the Sampling-Based Settling Time Circuit

Figures 10 through 12 underscore the importance of positioning the sampling window properly in time. In Figure 10 the sample gate delay initiates the sample window (trace A) too early and the residue amplifier's output (trace B) overdrives the oscilloscope when sampling commences. Figure 11 is better, with only slight off-screen activity. Figure 12 is optimal. All amplifier residue is well inside the screen boundaries.

Note 8: Achieving this level of performance also depends on layout. The circuit's construction involves a number of subtleties and is absolutely crucial. Please see Appendix G, "Breadboarding, Layout and Connection Techniques."

In general, it is good practice to "walk" the sampling window up to the last millivolt or so of amplifier slewing so that the onset of ring time is observable. The sampling based approach provides this capability and it is a very powerful measurement tool. Additionally, remember that

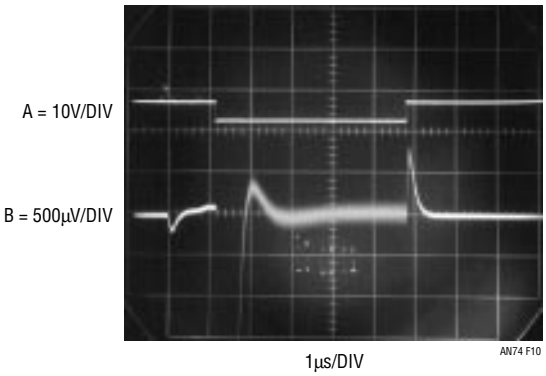

Figure 10. Oscilloscope Display with Inadequate Sample Gate Delay. Sample Window (Trace A) Occurs Too Early, Resulting in Off-Screen Activity in Settle Output (Trace B). Oscilloscope is Overdriven, Making Displayed Information Questionable

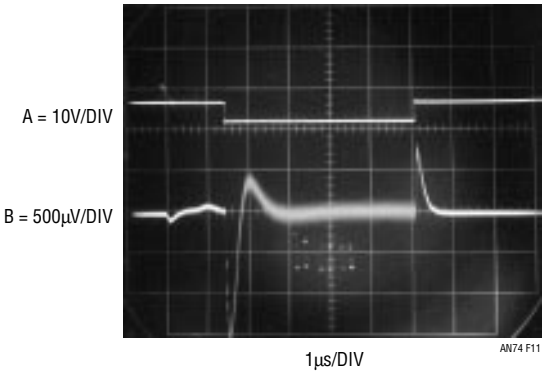

Figure 11. Increasing Sample Gate Delay Positions Sample Window (Trace A) So Settle Output (Trace B) Activity is On-Screen

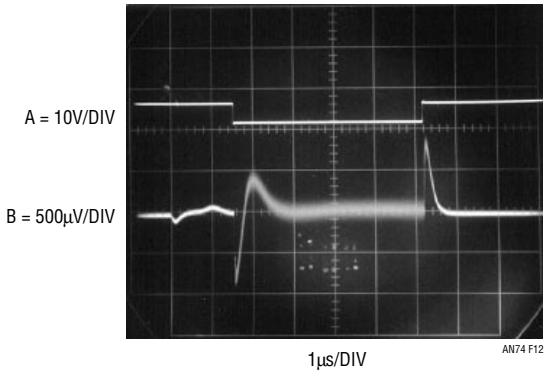

Figure 12. Optimal Sample Gate Delay Positions Sampling Window (Trace A) So All Settle Output (Trace B) Information is Well Inside Screen Boundaries

slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the 74H123 one-shot timing networks.

Compensation Capacitor Effects

The DAC amplifier requires frequency compensation to get the best possible settling time. The DAC has appreciable output capacitance, complicating amplifier response and making careful compensation capacitor selection even more important.[9] Figure 13 shows effects of very light compensation. Trace A is the time corrected input pulse and trace B the residue amplifier output. The light compensation permits very fast slewing but excessive ringing amplitude over a protracted time results. The ringing is so severe that it feeds through during a portion of the sample gate off-period, although no overdrive results. When sampling is initiated (just prior to the sixth vertical division) the ringing is seen to be in its final stages, although still offensive. Total settling time is about 2.8µs. Figure 14 presents the opposite extreme. Here a large value compensation capacitor eliminates all ringing but slows down the amplifier so much that settling stretches out to 3.3µs. The best case appears in Figure 15. This photo was taken with the compensation capacitor carefully chosen for the best possible settling time. Damping is tightly controlled and settling time goes down to 1.7µs.

Note 9: This section discusses frequency compensation of the DAC amplifier within the context of sampling-based settling time measurement. As such, it is necessarily brief. Considerably more detail is available later in the text and in Appendix D, "Practical Considerations for DAC-Amplifier Compensation."

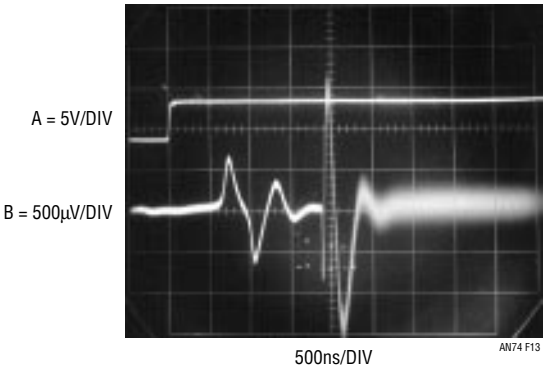

Figure 13. Settling Profile with Inadequate Feedback Capacitance Shows Underdamped Response. Excessive Ringing Feeds Through During Sample Gate Off-Period (Second Through ≈Sixth Vertical Divisions) But is Tolerable. t_{SETTLE} = 2.8µs

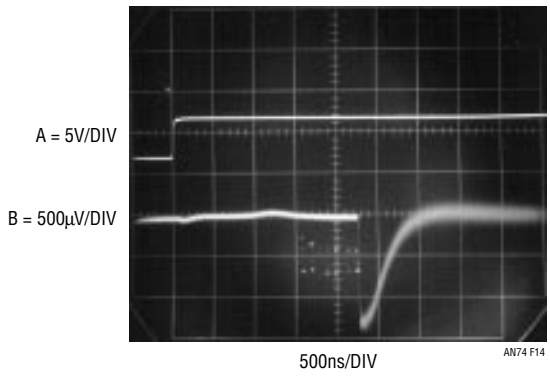

Figure 14. Excessive Feedback Capacitance Overdamps Response. t_{SETTLE} = 3.3µs

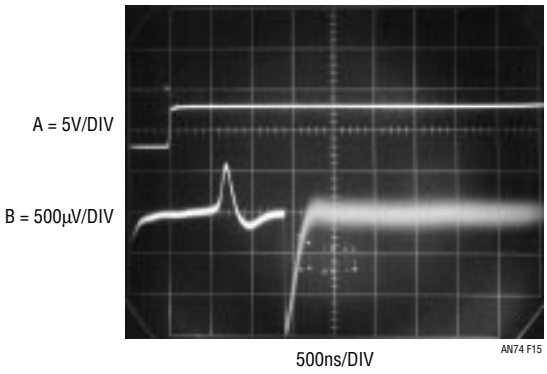

Figure 15. Optimal Feedback Capacitance Yields Tightly Damped Signature and Best Settling Time. t_{SETTLE} = 1.7µs

Verifying Results—Alternate Methods

The sampling-based settling time circuit appears to be a useful measurement solution. How can its results be tested to ensure confidence? A good way is to make the same measurement with alternate methods and see if results agree. To begin this exercise we return to the basic diode-bounded settle circuit.

Figure 16 repeats Figure 2's basic settling time measurement, with the same problem. The Schottky-bounded settle node forces a 400mV overdrive to the oscilloscope,

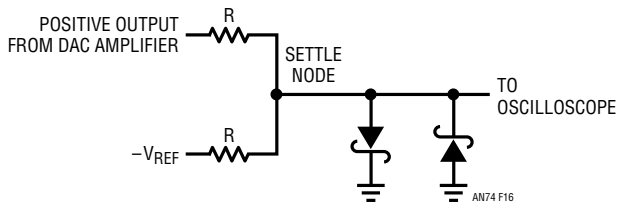

Figure 16. Clamped Settle Node Permits Oscilloscope Overdrive Because Diodes Have 400mV Drop

rendering all measurements useless. Now, consider Figure 17. This arrangement is similar, but the diodes are returned to bias voltages that are slightly lower than the diode drops. Theoretically, this has the same effect as ground-referred diodes with an inherently lower forward drop, greatly reducing oscilloscope overdrive. In practice, diode V-I characteristics and temperature effects limit achievable performance to uninteresting levels. Clamping reduction is minimal and diode forward leakage when the settle node reaches zero causes signal amplitude errors. Although impractical, this approach does hint at the way to a more useful method.

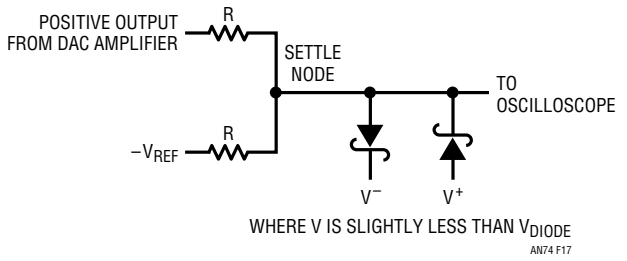

Figure 17. Biasing Diodes Theoretically Lowers Clamp Voltage. In Practice, V-I Characteristics and Temperature Effects Limit Performance

Alternate Method I—Bootstrapped Clamp

Figure 18's approach returns the diodes to amplifier-generated voltages bootstrapped from the settle-node input signal. In this way, the diode bias is actively maintained at the optimum point with respect to the signal to be clamped. During DAC amplifier slew, the settle-node signal is large and the amplifiers supply a resultant large bias to the diodes, forcing the desired small clamp voltage. When the DAC amplifier comes out of slew, the settle-node signal very nearly approaches zero, the amplifiers supply almost no diode bias and the oscilloscope monitors the uncorrupted settle node output. Adjustable amplifier gains permit optimal setting of positive and negative bound limits. This scheme offers the possibility of minimizing oscilloscope overdrive while preserving signal-path integrity.

A practical bootstrapped clamp appears in Figure 19. The actual clamp circuit, composed of A3 and A4, is nearly identical to the previous figure's theoretical incarnation. A1 and A2 are added, suppling a nonsaturating gain of 80 to the clamp. This permits a 500µV/DIV oscilloscope scale factor with respect to the DAC amplifier output. In Figure 20 the amplifier-bound voltages are set equal to the diode drops, and bootstrapping does not occur. The response is essentially identical to that of a simple diode clamp. In Figure 21 A4's gain is adjusted, reducing the positive clamp excursion. A3's gain is similarly trimmed in Figure 22, producing a corresponding reduction in the negative clamp limit. Note that in both photos, the small amplitude settle signal waveform (beginning about the fifth vertical division) is unaffected. Further refinement of the positive and negative trims produces Figure 23. The trims are optimized for minimal peak-to-peak amplitude while maintaining settle-signal waveform fidelity. This permits an oscilloscope running at 20mV/DIV (500µV at the DAC

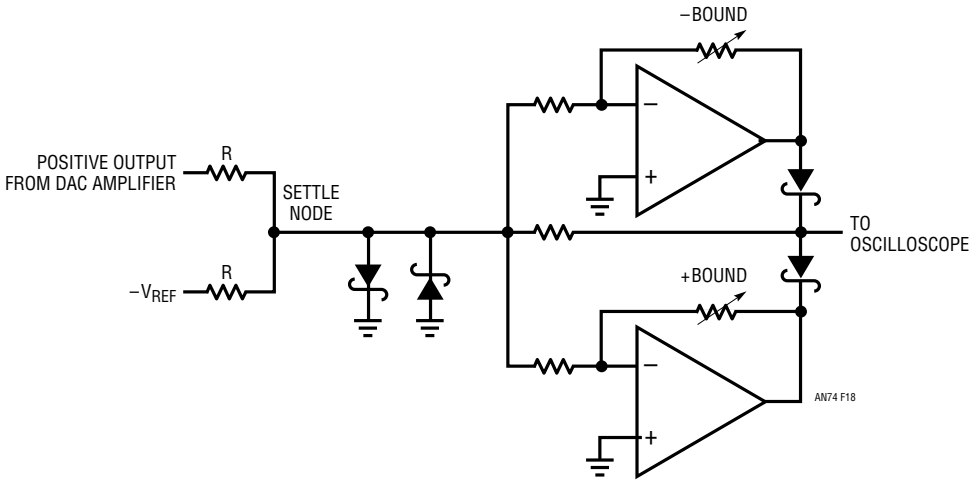

Figure 18. Conceptual Bootstrapped Clamp Biases Diodes From Input Signal, Minimizing Effects of V-I Characteristics and Temperature.

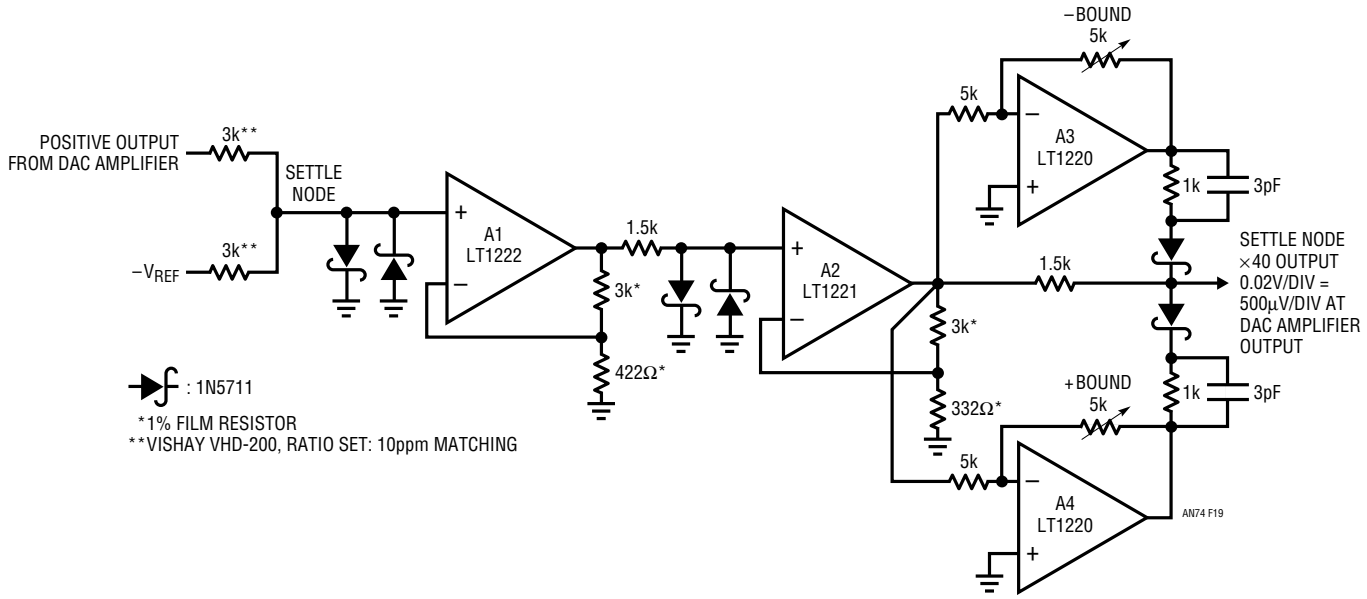

Figure 19. A Practical Bootstrapped Clamp. A1 and A2 Provide Gain to Bootstrapped Section. Positive and Negative Bounds are Adjustable

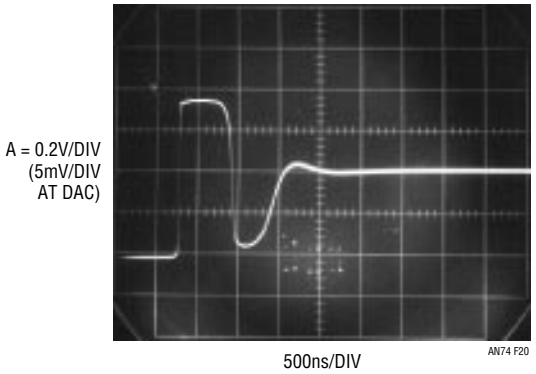

Figure 20. Bootstrapped Clamp Waveform with Bound Limits Equal to Diode Drops. Bootstrap Action Does Not Occur. Response is Identical to Diode Clamp

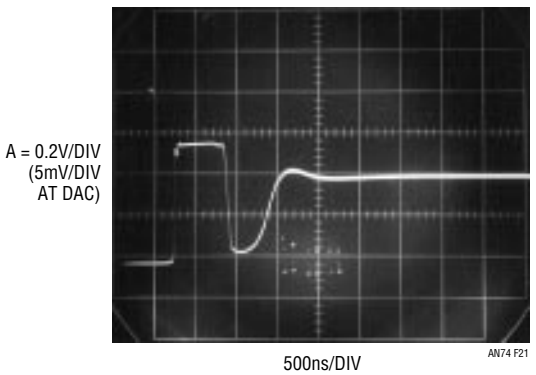

Figure 21. The Positive Bound is Adjusted, Reducing Positive Clamp Excursion

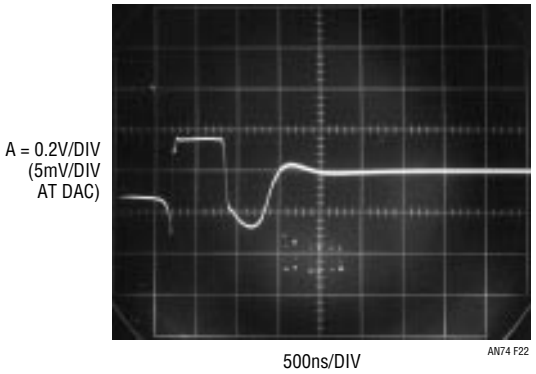

Figure 22. The Negative Bound is Trimmed, Reducing Negative Clamp Limit

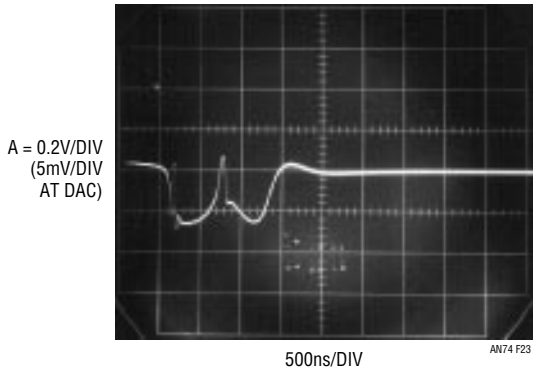

Figure 23. Positive and Negative Bound Adjustments are Optimized for Minimal Peak-to-Peak Amplitude. Waveform Information in Settling Region (Right of Fourth Vertical Division) is Undistorted and Identical to Figure 20

amplifier) to monitor the settle signal with only a 2.5× overdrive. This is not as ideal a situation as the sampling approach, which has no overdrive, but is markedly improved over the simple diode clamp. The monitoring oscilloscope selected must be verified to produce reliable displays while withstanding the 2.5× overdrive.[10]

Figure 24 shows the bootstrapped clamp adapted to Figure 6's settling-time test circuit. The settle node feeds the residue amplifier, which drives the bootstrapped clamp. As before, the input pulse is time corrected for signal path delays.[11] Additionally, similar type FET probes at the outputs ensure overall delay matching.[12] Figure 25 shows the results. Trace A is the time-corrected input step and trace B the settle signal. The oscilloscope undergoes about a 2.5× overdrive, although the settling signal appears undistorted.

Note 10: This limitation is surmountable by improving the bootstrapped clamp's dynamic operating range. Future work will be directed towards this end. For the present, the following oscilloscopes have been found to produce faithful results under the 2.5× overdrive conditions noted in the text. The instruments include Tektronix types 547 and 556 (type 1A1 or 1A4 plug-in) and types 453, 454, 453A and 454A. See also Appendix B, "Evaluating Oscilloscope Overload Performance."

Note 11: Characterization of signal path delay is treated in Appendix C, "Measuring and Compensating Residue Amplifier Delay."

Note 12: The bootstrapped clamp's output impedance mandates a FET probe. A second FET probe monitors the input step, but only to maintain channel delay matching.

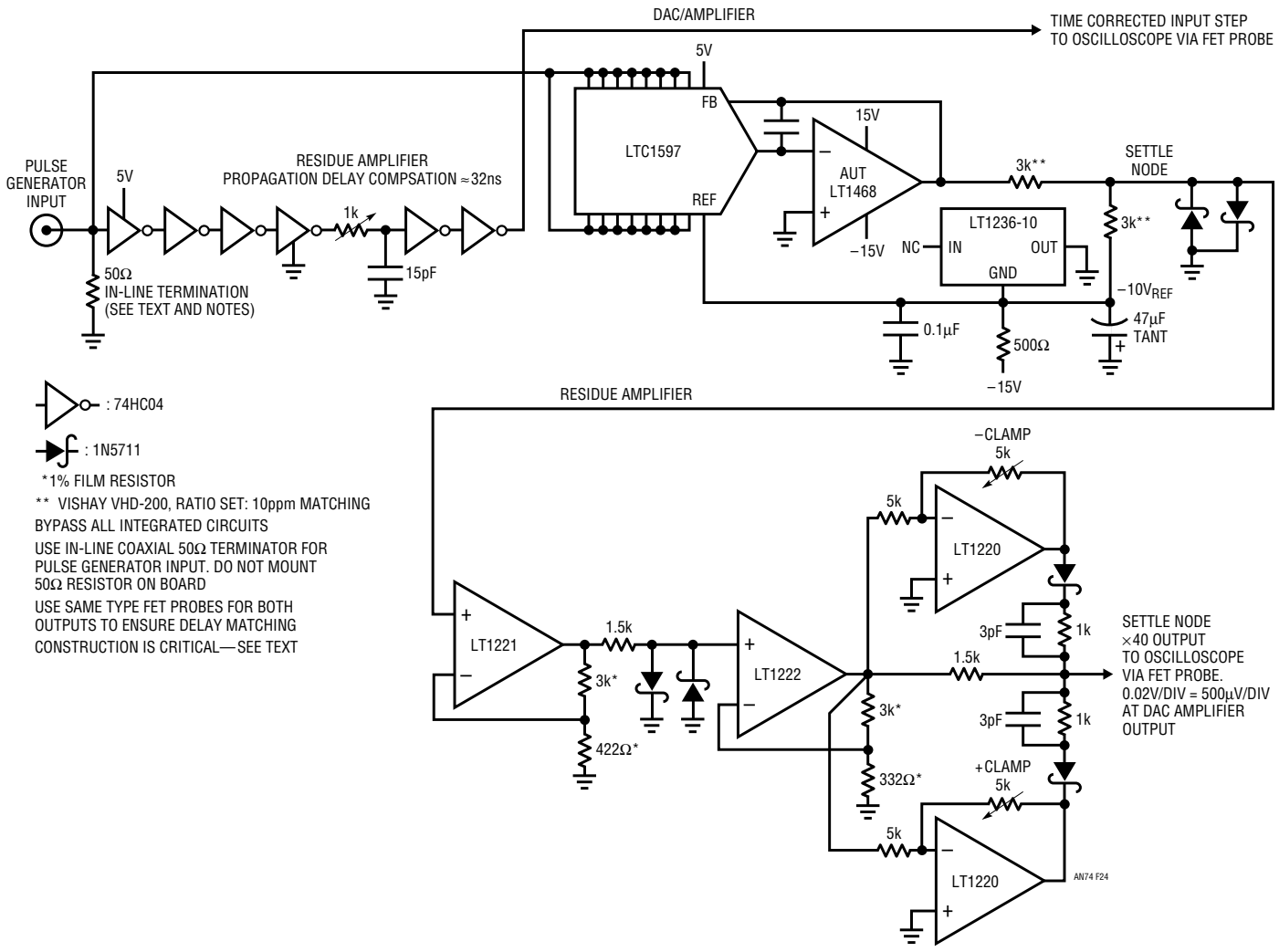

Figure 24. Complete Bootstrapped Clamp-Based DAC Settling Time Measurement Circuit. Overdrive is Substantially Reduced Over Conventional Diode Clamp, But Oscilloscope Must Tolerate ≈2.5× Screen Overdrive

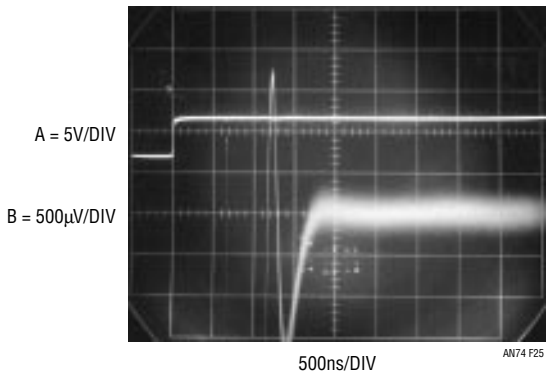

Figure 25. The Bootstrapped Clamp-Amplifier Measuring Settling Time. Oscilloscope Must Tolerate 2.5× Screen Overdrive for Meaningful Results

Alternate Method II—Sampling Oscilloscope

It was stated earlier that classical sampling oscilloscopes were inherently immune to overdrive.[13] If this is so, why not utilize this feature and attempt settling time measurement with a simple diode clamp? Figure 26 does this. The schematic is identical to Figure 24 except that the bootstrapped clamp has been replaced with a simple diode clamp. Under these conditions the sampling 'scope[14] is heavily overdriven, but is ostensibly immune to the insult. Figure 27 puts the sampling oscilloscope to the test. Trace A is the time corrected input pulse and trace B the settle signal. Despite a brutal overdrive, the 'scope appears to respond cleanly, giving a very plausible settle signal presentation.

Note 13: See Appendix B, "Evaluating Oscilloscope Overdrive Performance," for in-depth discussion.

Note 14: Tektronix type 661 with 4S1 vertical and 5T3 timing plug-ins.

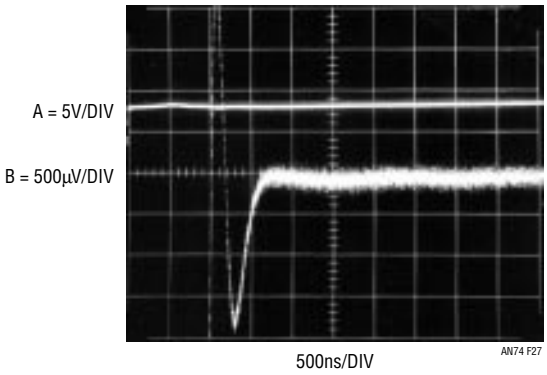

Figure 27. DAC Settling Time Measurement with the Classical Sampling 'Scope. Oscilloscope's Overload Immunity Permits Accurate Measurement Despite Extreme Overdrive

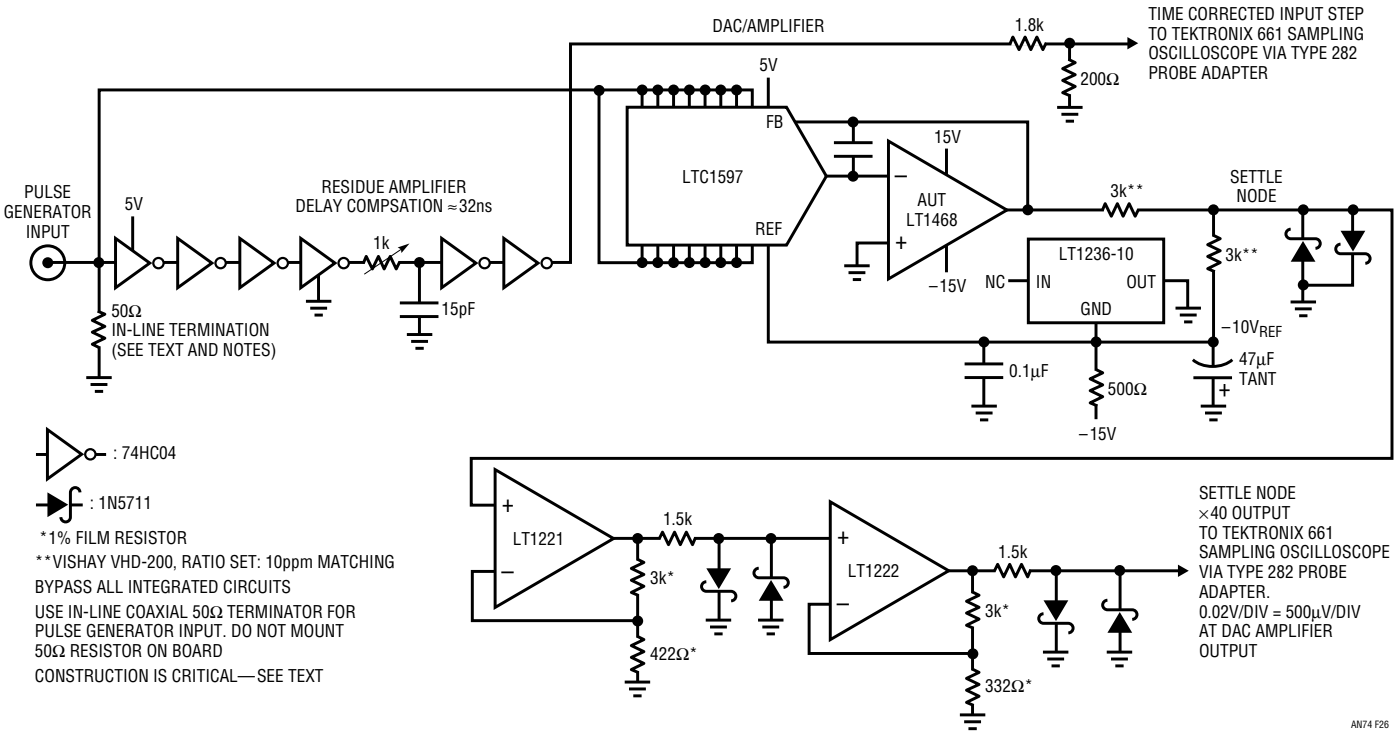

Figure 26. DAC Settling Time Test Circuit Using Classical Sampling Oscilloscope. Circuit is Similar to Figure 24. Sampling 'Scope's Inherent Overload Immunity Eliminates Bootstrapped Clamp Requirement

Alternate Method III—Differential Amplifier

In theory, a differential amplifier with one input biased at the expected settled voltage can measure settling time to 16-bit resolution. In practice, this is an extraordinarily demanding measurement for a differential amplifier. The amplifier's overload recovery characteristics must be pristine. In fact, no commercially produced differential amplifier or differential oscilloscope plug-in has been available that meets this requirement. Recently, an instrument has appeared that, although not fully specified at these levels, appears to have superb overload recovery performance. Figure 28 shows the differential amplifier (type and manufacturer appear in the schematic notes) monitoring the DAC output amplifier. The amplifier's negative input is biased from its internal adjustable reference to the expected settled voltage. The diff. amp's clamped output, operating at a gain of 10, feeds A1-A2, a bounded, nonsaturating gain of 40. Note that the monitoring oscilloscope, operating at 0.2V/DIV (500µV/DIV at the DAC amplifier) cannot be overdriven. Figure 29 shows the results. Trace A is the time corrected input step and trace B the settle signal. The settle signal is seen to come smoothly out of bound, entering the amplified linear region between the third and fourth vertical divisions. The settling signature appears reasonable and complete settling occurs just beyond the fourth vertical division.

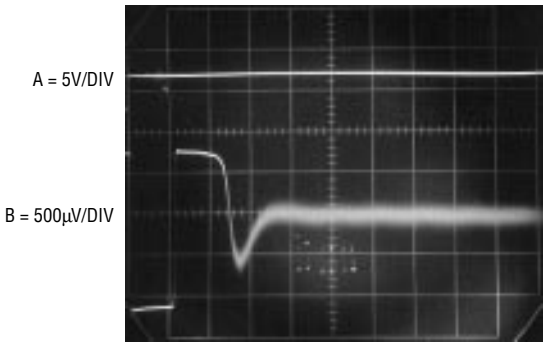

Figure 29. DAC Settling Time Measurement with the Differential/ Clamped Amplifiers. All Oscilloscope Input Signal Excursions are On-Screen.

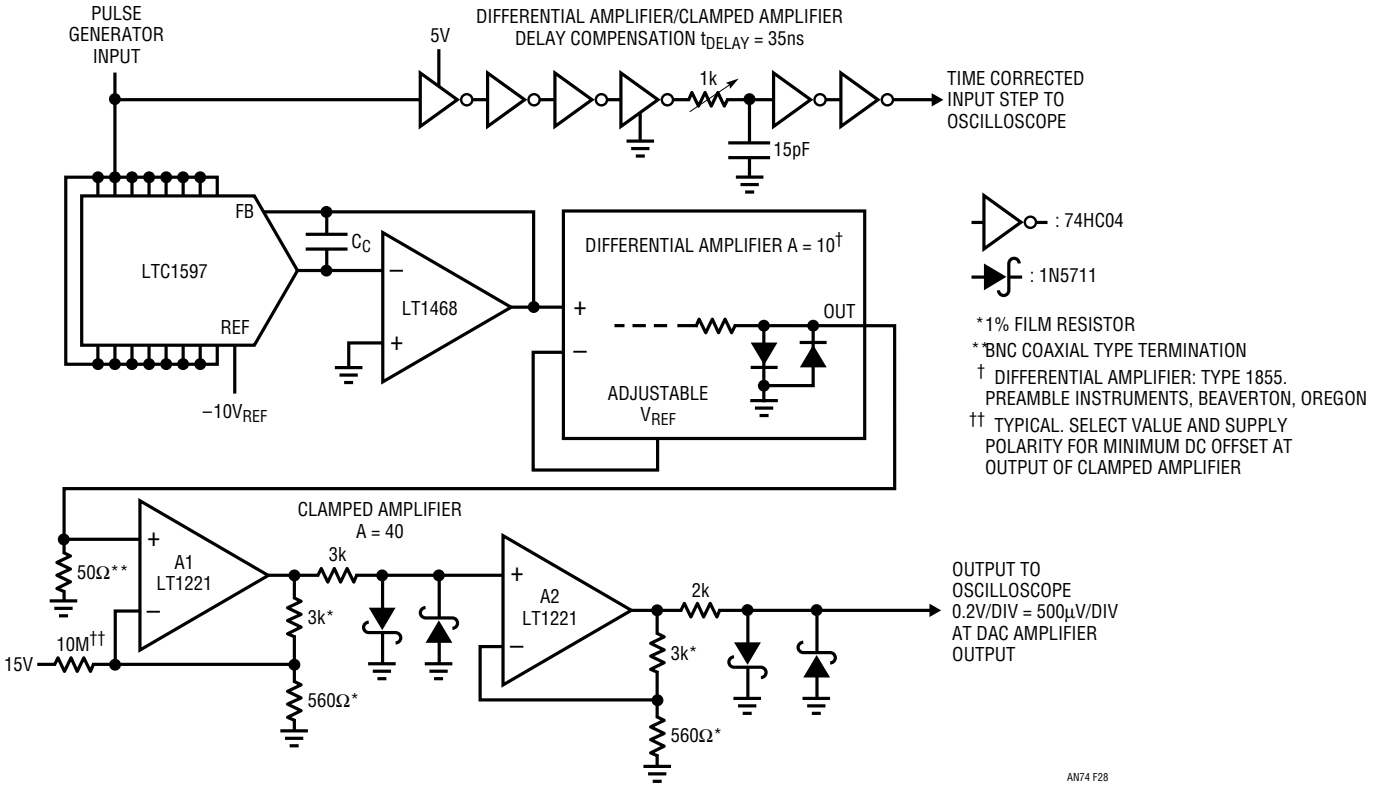

Figure 28. Settling Time Measurement Using a Differential Amplifier. Amplifier Must Have Excellent Input Overload Recovery. Clamped Amplifier's Bounded Gain Stages Limit Amplitude While Maintaining Linear Region Operation. Oscilloscope is Not Overdriven

Summary of Results

The simplest way to summarize the four different method's results is by visual comparison. Figures 30 through 33 repeat previous photos of the four different settling-time methods. If all four approaches represent good measurement technique and are constructed properly, results should be indentical.[15] If this is the case, the identical data produced by the four methods has a high probability of being valid.

Examination of the four photographs shows identical 1.7µs settling times and settling waveform signatures. The shape of the settling waveform, in every detail, is identical in all four photos. This kind of agreement provides a high degree of credibility to the measured results. It also provides the confidence necessary to characterize a wide variety of amplifiers. Figure 34 lists various LTC amplifiers and their measured settling times to 16 bits.

About This Chart

The writer despises charts. In their attempt to gain authority they simplify, and glib simplification is the host of mother nature's surprise party. Any topic as complex as DAC-amplifier settling time to 16 bits is a dangerous place for oversimplification. There are simply too many variables and exceptions to accommodate the categorical statement a chart implies. It is with these reservations that Figure 34 is presented.[16] The chart lists measured settling times to 16 bits for various LTC amplifiers used with the LTC1595-7 16-bit DACs. A number of conditions and comments apply to interpreting the chart's information.

Note 15: Construction details of the settling time fixtures discussed here appear (literally) in Appendix G, "Breadboarding, Layout and Connection Techniques."

Note 16: Readers detecting author ambivalence about the inclusion of Figure 34's chart are not hallucinating.

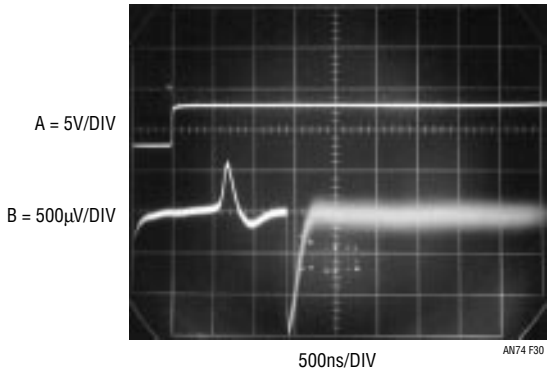

Figure 30. DAC Settling Time Measurement Using the Sampling Bridge Circuit. t_{SETTLE} = 1.7µs

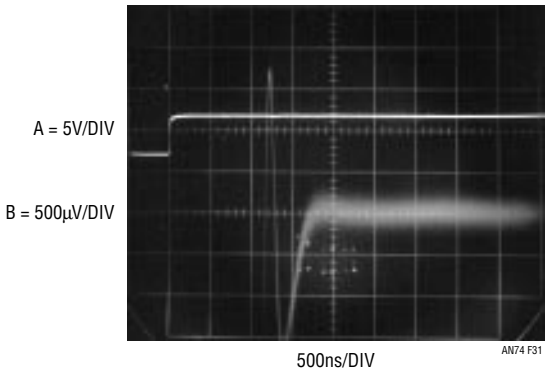

Figure 31. DAC Settling Time Measurement with the Bootstrapped Clamp Method. t_{SETTLE} = 1.7µs

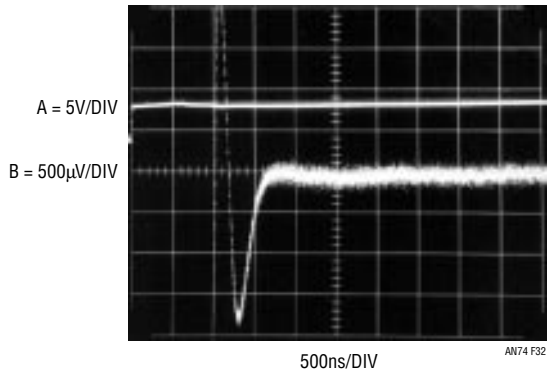

Figure 32. DAC Settling Time Measurement Using the Classical Sampling 'Scope. t_{SETTLE} = 1.7µs

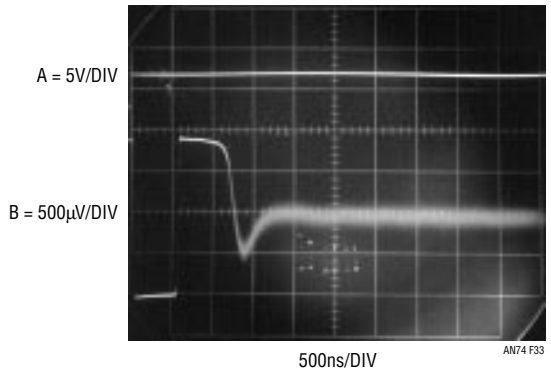

Figure 33. DAC Settling Time Measurement with the Differential Amplifier. t_{SETTLE} = 1.7µs

DAC Settling Time Measurement Using Four Different Methods. Waveform Signatures and Settling Times Appear Identical

AMPLIFIER	OPTIMIZED SETTLING TIME AND TYPICAL COMPENSATION VALUE		CONSERVATIVE SETTLING TIME AND COMPENSATION VALUE		COMMENTS
LT1001	65µs	100pF	120µs	100pF	Good Low Speed Choice
LT1006	26µs	66pF	50µs	150pF	
LT1007	17µs	100pF	19µs	100pF	I_B Gives ≈1LSB Error at 25°C
LT1008	64µs	100pF	115µs	100pF	
LT1012	56µs	75pF	116µs	75pF	Good Low Speed Choice
LT1013	50µs	150pF	75µs	150pF	≈1LSB Error Due to V_{OS} over Temperature
LT1055	3.7µs	54pF	5µs	75pF	V_{OS} Gives ≈2 to 3LSB Error over Temperature
LT1077	110µs	100pF	200µs	100pF	
LT1097	60µs	75pF	120µs	75pF	Good Low Speed Choice
LT1122	3µs	51pF	3.5µs	68pF	V_{OS} Induced Errors
LTC1150	7ms	100pF	10ms	100pF	Special Case. See Appendix E. Needs Output Booster, e.g., LT1010
LT1178	330µs	100pF	450µs	100pF	
LT1179	330µs	100pF	450µs	100pF	
LT1211	5.5µs	73pF	6.5µs	82pF	I_B and V_{OS} Based Errors
LT1213	4.6µs	58pF	5.8µs	68pF	I_B and V_{OS} Based Errors
LT1215	3.6µs	53pF	4.7µs	68pF	I_B and V_{OS} Based Errors
LT1218	110µs	100pF	200µs	100pF	≈1.5LSB Error Due to V_{OS}. ≈4 to 5LSB I_B Based Errors
LT1220	2.3µs	41pF	3.1µs	56pF	V_{OS} and I_B Based Errors
LT1366	64µs	100pF	100µs	150pF	V_{OS} and I_B Based Errors
LT1413	45µs	100pF	75µs	120pF	≈2LSB Error Due to V_{OS}
LT1457	7.4µs	100pF	12µs	120pF	5 to 6LSB Error From V_{OS} over Temperature
LT1462	78µs	100pF	130µs	120pF	7 to 8LSB Error Due to V_{OS} over Temperature
LT1464	19µs	90pF	30µs	110pF	See LT1462 Comments Above
LT1468	1.7µs	20pF	2.5µs	30pF	Fastest Settling with 16-Bit Performance
LT1490	175µs	100pF	300µs	100pF	V_{OS} Based Errors
LT1492	7.5µs	80pF	10µs	100pF	V_{OS} and I_B Based Errors
LT1495	10ms	100pF	25ms	100pF	Measured with Hourglass and Differential Voltmeter. Needs Output Booster, e.g., LT1010
LT1498	5µs	60pF	7.3µs	82pF	V_{OS} and I_B Based Errors
LT1630	4.5µs	63pF	6.7µs	82pF	Significant I_B Based Error
LT1632	4µs	55pF	5.2µs	68pF	Significant I_B Based Error
LTC1650	6µs		7.3µs		DAC On-Board. ±4V Step. ≈10LSB V_{OS} Related Error Over Temperature
LT2178	330µs	100pF	450µs	100pF	1 to 2LSB V_{OS} Based Error

Figure 34. 16-Bit Settling Time for Various Amplifiers Driven by the LT1597 DAC. Optimized Settling Times Require Trimming Compensation Capacitor, Conservative Times are Untrimmed. LT1468 (Shaded) Offers Fastest Settling Time While Maintaining Accuracy Over Temperature

The amplifiers selected are not all accurate to 16 bits over temperature, or (in some cases) even at 25°C. However, many applications, such as AC signal processing, servo loops or waveform generation, are insensitive to DC offset error and, as such, these amplifiers are worthy candidates. Applications requiring DC accuracy to 16 bits (10V full scale) must keep input errors below 15nA and 152µV to maintain performance.

The settling times are quoted for "optimized" and "conservative" cases. The optimized case uses a typical amplifier-DAC combination. This implies "design centered" values for amplifier slew rate and DAC output resistance and capacitance. It also permits trimming the amplifier's feedback capacitor to obtain the best possible settling time. The conservative category assumes worst-case amplifier slew rate, highest DAC output impedances and untrimmed, standard 5% feedback capacitors. This worst-case error summation is perhaps unduly pessimistic; RMS summing may represent a more realistic compromise. However, such a maudlin outlook helps avoid unpleasant surprises in production. Settling times are quoted using ±15V supplies, a –10V DAC reference and a 10V positive output step. The sole exception to this is the LTC1650, a 16-bit DAC with amplifier onboard. This device is powered by ±5V supplies and settling is measured with a 4V reference and a ±4V swing.[17] All feedback capacitances listed were determined with a General Radio model 1422-CL precision variable air capacitor.[18]

In general, the slower amplifiers' extended slew times make their ring times vanishingly small settling-time contributors. This is reflected in identical feedback capacitor values for the optimized and conservative cases. Conversely, faster amplifiers' ring times are significant terms, resulting in different compensation values for the two categories. Additional considerations for compensation are discussed in Appendix D, "Practical Considerations for DAC-Amplifier Compensation."

Note 17: See Appendix F, "Settling Time Measurement of Serially Loaded DACs."

Note 18: A thing of transcendent beauty. It is worth owning this instrument just to look at it. It is difficult to believe humanity could fashion anything so perfectly gorgeous.

Thermally Induced Settling Errors

A final category of settling-time error is thermally based. Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed it is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Figure 35 shows such a tail. The amplifier slowly (note horizontal sweep speed) drifts 200µV after settling has apparently occurred. Often, the thermal tail's effect can be accentuated by loading the amplifier's output. Figure 36 doubles the error by increasing amplifier loading.

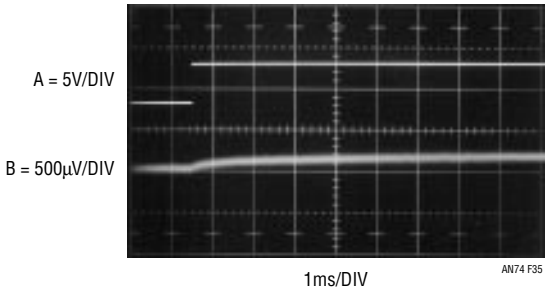

Figure 35. Typical Thermal Tail in a Poorly Designed Amplifier. Device Drifts 200µV (>1LSB) After Settling Apparently Occurs

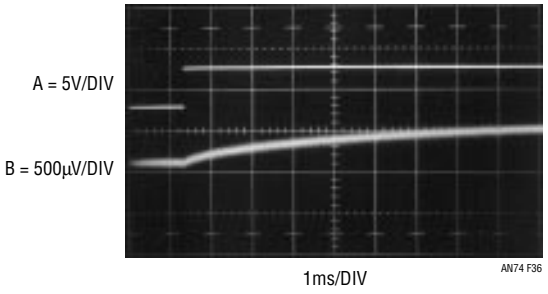

Figure 36. Loading the Amplifier Increases Thermal Tail Error to 400µV (>2.5LSB)

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APPENDIX A

A HISTORY OF HIGH ACCURACY DIGITAL-TO-ANALOG CONVERSION

People have been converting digital-to-analog quantities for a long time. Probably among the earliest uses was the summing of calibrated weights (Figure A1, left center) in weighing applications. Early electrical digital-to-analog conversion inevitably involved switches and resistors of different values, usually arranged in decades. The application was often the calibrated balancing of a bridge or reading, via null detection, some unknown voltage. The most accurate resistor-based DAC of this type is Lord Kelvin's Kelvin-Varley divider (Figure, large box). Based on switched resistor ratios, it can achieve ratio accuracies of 0.1ppm (23+ bits) and is still widely employed in standards laboratories. High speed digital-to-analog conversion resorts to electronically switching the resistor network. Early electronic DACs were built at the board level using discrete precision resistors and germanium transistors (Figure, center foreground, is a 12-bit DAC from a Minuteman missile D-17B inertial navigation system, circa 1962). The first electronically switched DACs available as standard product were probably those produced by Pastoriza Electronics in the mid 1960s. Other manufacturers followed and discrete- and monolithically-based modular DACs (Figure, right and left) became popular by the 1970s. The units were often potted (Figure, left) for ruggedness, performance or to (hopefully) preserve proprietary knowledge. Hybrid technology produced smaller package size (Figure, left foreground). The development of Si-Chrome resistors permitted precision monolithic DACs such as the LTC1595 (Figure, immediate foreground). In keeping with all things monolithic, the cost-performance trade off of modern high resolution IC DACs is a bargain. Think of it! A 16-bit DAC in an 8-pin IC package. What Lord Kelvin would have given for a credit card and LTC's phone number.

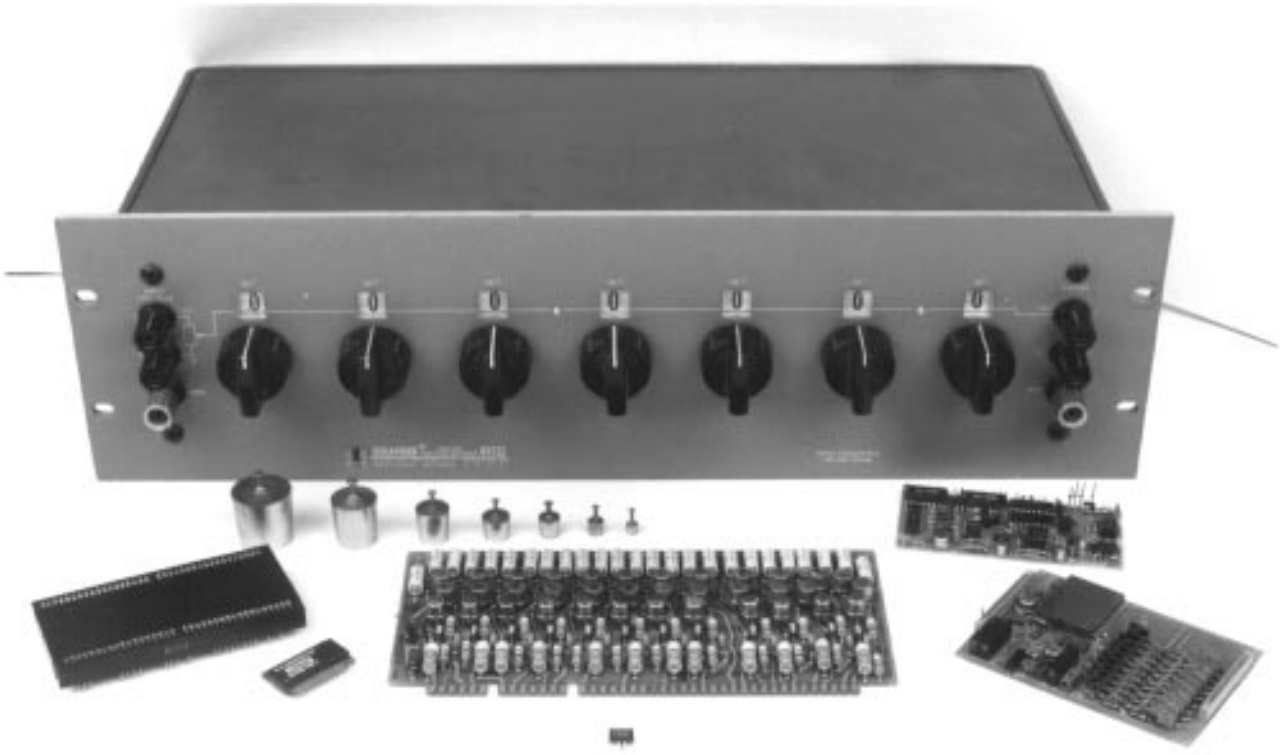

Figure A1. Historically Significant Digital-to-Analog Converters Include: Weight Set (Center Left), 23+ Bit Kelvin-Varley Divider (Large Box), Hybrid, Board and Modular Types, and the LTC1595 IC (Foreground). Where Will It All End?

APPENDIX B

EVALUATING OSCILLOSCOPE OVERDRIVE PERFORMANCE

Most of the settling-time circuits are heavily oriented towards providing little or no overdrive to the monitoring oscilloscope. This is done to avoid overdriving the oscilloscope. Oscilloscope recovery from overdrive is a grey area and almost never specified. Some of the settling time measurement methods require the oscilloscope to be overdriven. In these cases, the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overdrive before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overdrive, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overdrive varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100× overload at 0.005V/DIV may be very different than at 0.1V/DIV. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overdrive must be approached with caution.

Why do most oscilloscopes have so much trouble recovering from overdrive? The answer to this question requires some study of the three basic oscilloscope types' vertical paths. The types include analog (Figure B1A), digital (Figure B1B) and classical sampling (Figure B1C) oscilloscopes. Analog and digital 'scopes are susceptible to overdrive. The classical sampling 'scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope (Figure B1A) is a real time, continuous linear system.[1] The input is applied to an attenuator, which is unloaded by a wideband buffer. The vertical preamp provides gain, and drives the trigger pick-off, delay line and the vertical output amplifier. The attenuator and delay line are passive elements and require little comment. The buffer, preamp and vertical output amplifier are complex linear gain blocks, each with dynamic operating range restrictions. Additionally, the operating point of each block may be set by inherent circuit balance, low frequency stabilization paths or both. When the input is overdriven, one or more of these stages may saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may require surprising lengths of time.[2]

The digital sampling oscilloscope (Figure B1B) eliminates the vertical output amplifier, but has an attenuator buffer and amplifiers ahead of the A/D converter. Because of this, it is similarly susceptible to overdrive recovery problems.

The classical sampling oscilloscope is unique. Its nature of operation makes it inherently immune to overload. Figure B1C shows why. The sampling occurs *before* any gain is taken in the system. Unlike Figure B1B's digitally sampled 'scope, the input is fully passive to the sampling point. Additionally, the output is fed back to the sampling bridge, maintaining its operating point over a very wide range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a wide range of oscilloscope inputs. Because of all this, the amplifiers in this instrument do not see overload, even at 1000× overdrives, and there is no recovery problem. Additional immunity derives from the instrument's relatively slow sample rate—even if the amplifiers were overloaded, they would have plenty of time to recover between samples.[3]

The designers of classical sampling 'scopes capitalized on the overdrive immunity by including variable DC offset generators to bias the feedback loop (see Figure B1C, lower right). This permits the user to offset a large input, so small amplitude activity on top of the signal can be accurately observed. This is ideal for, among other things, settling time measurements. Unfortunately, classical sampling oscilloscopes are no longer manufactured, so if you have one, take care of it!

Note 1: Ergo, the Real Thing. Hopelessly bigoted residents of this locale mourn the passing of the analog 'scope era and frantically hoard every instrument they can find.

Note 2: Some discussion of input overdrive effects in analog oscilloscope circuitry is found in reference 10.

Note 3: Additional information and detailed treatment of classical sampling oscilloscope operation appears in references 14-17 and 20-22.

Although analog and digital oscilloscopes are susceptible to overdrive, many types can tolerate some degree of this abuse. The early portion of this appendix stressed that measurements involving oscilloscope overdrive must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity that eliminates all off-screen activity. Figure B2 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure B3) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original

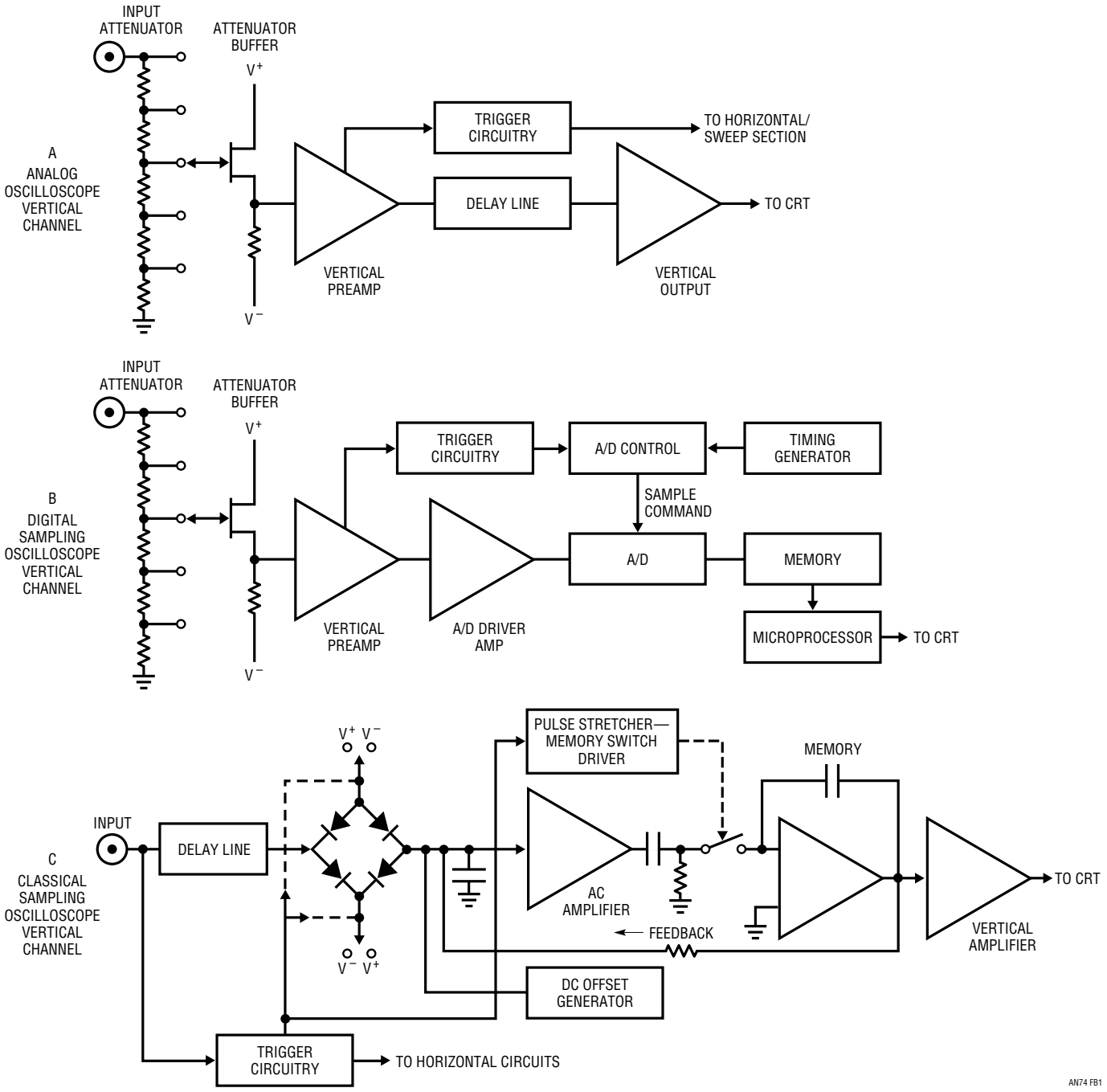

Figure B1. Simplified Vertical Channel Diagrams for Different Type Oscilloscopes. Only the Classical Sampling 'Scope (C) Has Inherent Overdrive Immunity. Offset Generator Allows Viewing Small Signals Riding On Large Excursions

display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure B4, gain has been further increased, and all the features of Figure B3 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure B5 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure B4. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure B6 the

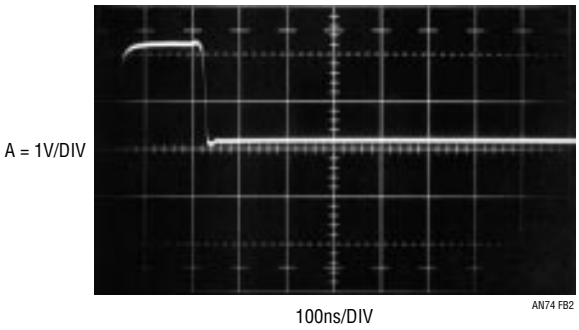

Figure B2

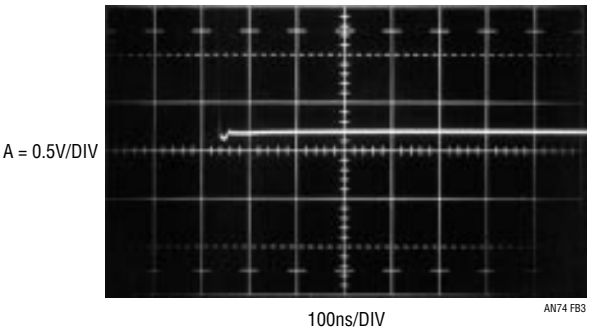

Figure B3

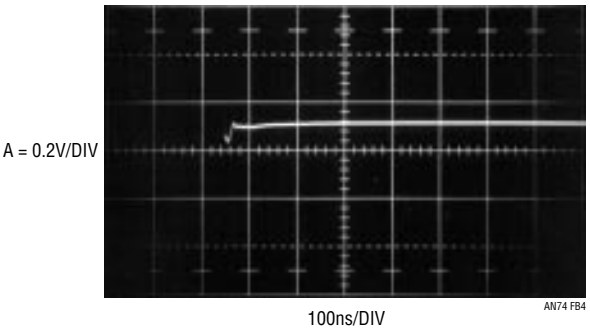

Figure B4

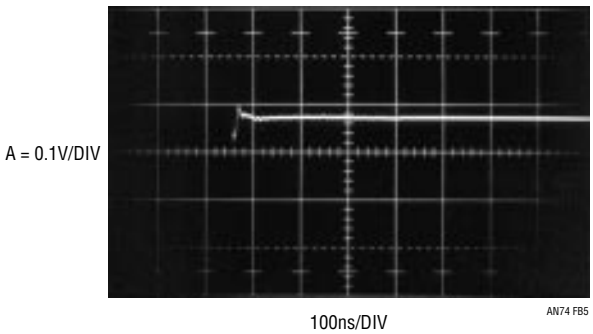

Figure B5

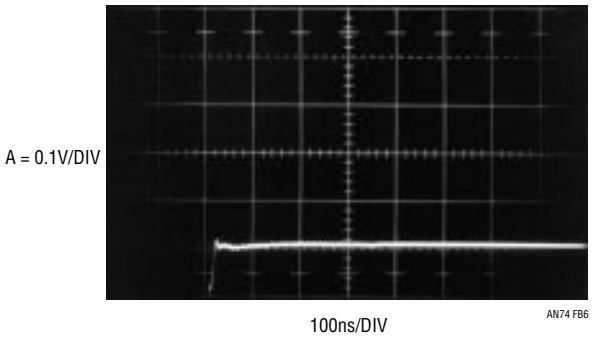

Figure B6

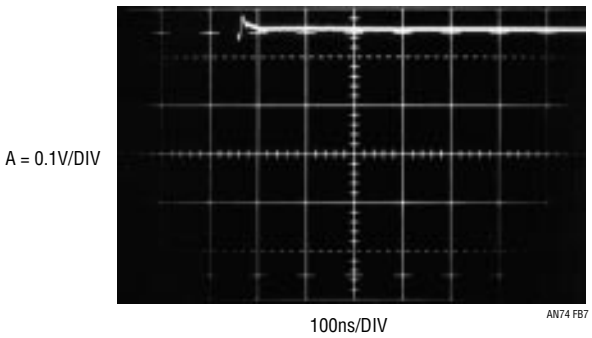

Figure B7

Figures B2-B7. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure B7). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

APPENDIX C

MEASURING AND COMPENSATING RESIDUE-AMPLIFIER DELAY

The settling-time circuits utilize an adjustable delay network to time correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of a few percent, so a first-order correction is adequate. Setting the delay trim involves observing the network's input-output delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex. Measuring the sampling bridge-based circuit's signal path delay involves modifications to Figure 6, shown in Figure C1. These changes lock the circuit into its "sample" mode, permitting an input-to-output delay measurement under signal-level conditions similar to normal operation. In Figure C2, trace A is the pulse-generator input at 200μV/DIV (note 10k-1Ω divider feeding the settle node). Trace B shows the circuit output at A2, delayed by about 12ns. This delay is a small error, but is readily corrected by adjusting the delay network for the same time lag.

Figure C3 takes a similar approach with Figure 26's sampling 'scope-based measurement. Modifications permit a small amplitude pulse to drive the settle node, mimicking normal operation signal level conditions. Circuit output at A2 is monitored for delay with respect to the input pulse. Note that A2's high impedance output requires a FET probe to avoid loading. As such, the input pulse must be routed to the oscilloscope via a similar FET probe to maintain delay matching. Figure C4 shows results. The output (trace B) lags the input by 32ns. This factor is used to calibrate text Figure 26's delay network, compensating the circuit's signal path propagation time error.

Delay compensation values for the bootstrapped clamp (text Figure 24) and differential amplifier (text Figure 28) circuits were determined in similar fashion.

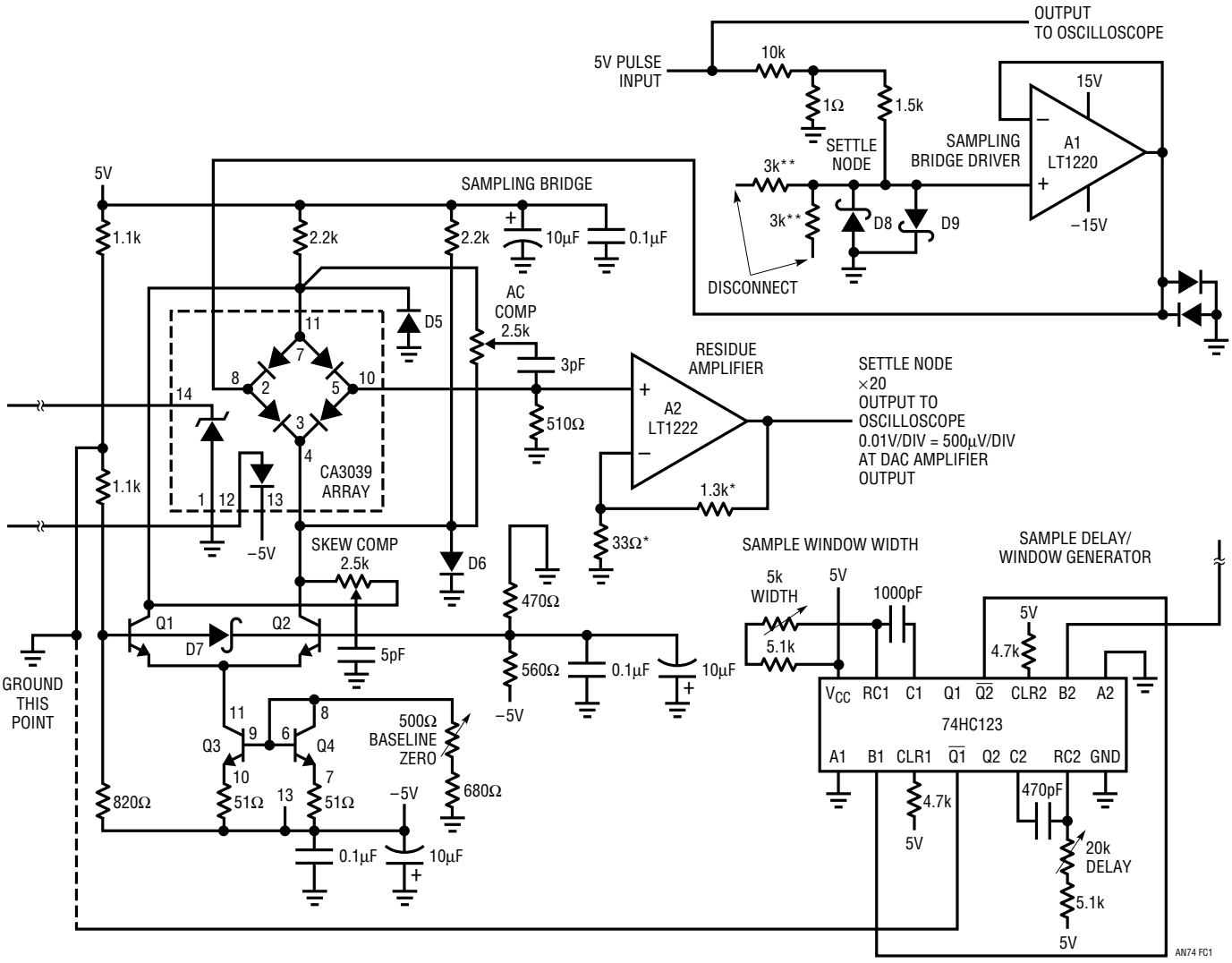

Figure C1. Sampling Bridge Circuit Modifications for Measuring Amplifier Delay. Changes Lock Circuit into Sample Mode, Permitting Input-to-Output Delay Measurement

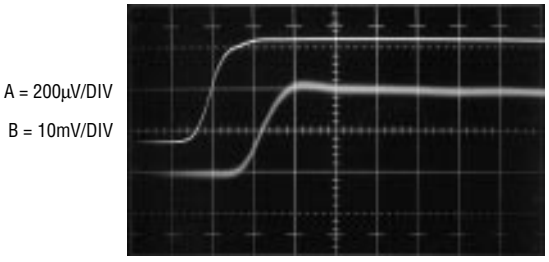

Figure C2. Input-Output Delay for Sampling Bridge Circuit Measures About 12ns

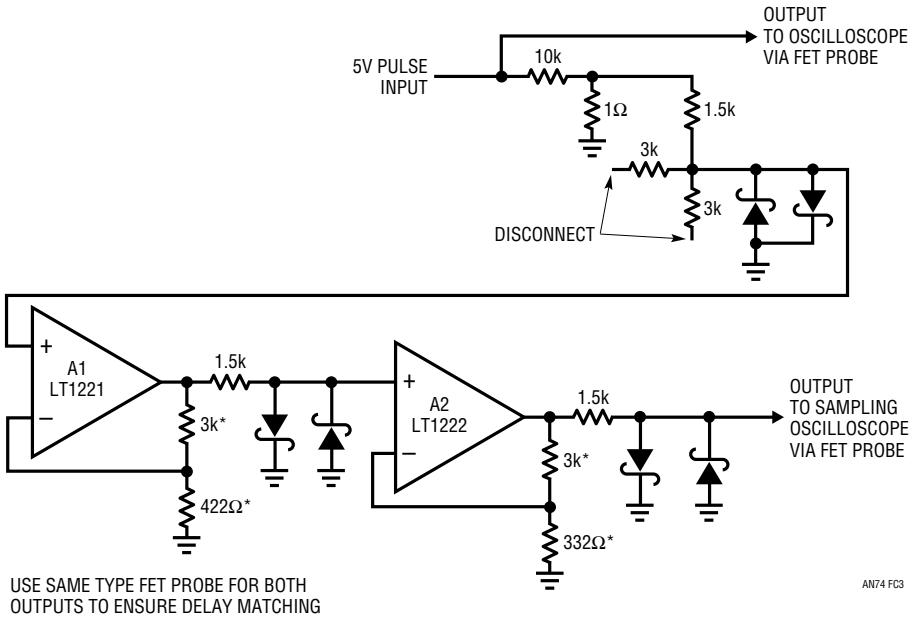

Figure C3. Partial Version of Figure 26 Showing Modifications Permitting Delay Time Measurment. FET Probes are the Same Type, Eliminating Time Skewing Error

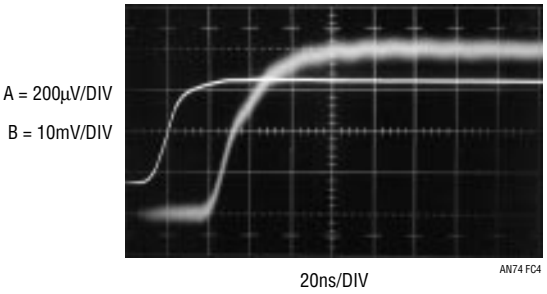

Figure C4. Delay Measurement Results for Figure C3. Input-Output Time Lag is About 32ns

APPENDIX D

PRACTICAL CONSIDERATIONS FOR DAC-AMPLIFIER COMPENSATION

There are a number of practical considerations in compensating the DAC-amplifier pair to get fastest settling time. Our study begins by revisiting text Figure 1 (repeated here as Figure D1). Settling time components include delay, slew and ring times. Delay is due to propagation time through the DAC-amplifier and is a very small term. Slew time is set by the amplifier's maximum speed. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. Once a DAC-amplifier pair have been chosen, only ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the fastest slewing amplifier available to obtain best settling. Unfortunately, fast slewing amplifiers usually have extended ring times, negating their brute force speed advantage. The penalty for raw speed is, invariably, prolonged ringing, which can only be damped with large compensation capacitors. Such compensation works, but results in protracted settling times. The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and compensate it properly. This is harder than it sounds because amplifier settling time cannot be predicted or extrapolated from any combination of data sheet specifications. It must be measured in the intended configuration. In the case of a DAC-amplifier, a number of terms combine to influence settling time. They include amplifier slew rate and AC dynamics, DAC output resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous.[1] If the DAC's parasitics are eliminated and replaced with a pure resistive source, amplifier settling time is still not readily predictable. The DAC's output impedance terms just make a difficult problem more messy. The only real handle available to deal with all this is the feedback compensation capacitor, C_F. C_F's purpose is to roll off amplifier gain at the frequency that permits best dynamic response. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the DAC's parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, typically 100pF, and it varies with code.

Best settling results when the compensation capacitor is selected to functionally compensate for all the above parasitics. Figure D2 shows results for an optimally selected feedback capacitor. Trace A is the DAC input pulse and trace B the amplifier's settle signal. The amplifier is seen to come cleanly out of slew (sample gate opens just prior to fifth vertical division) and settle very quickly.

Note 1: Spice aficionados take notice.

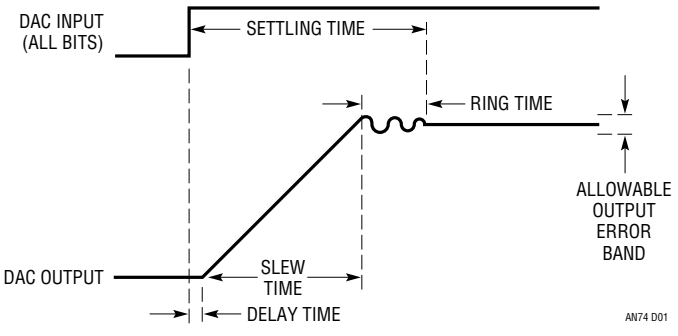

Figure D1. DAC-Amplifier Settling Time Components Include Delay, Slew and Ring Times. For Given Components, Only Ring Time is Readily Adjustable

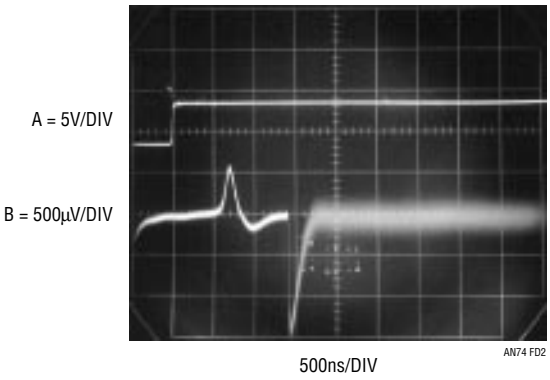

Figure D2. Optimized Compensation Capacitor Permits Nearly Critically Damped Response, Fastest Settling Time. t_{SETTLE} = 1.7μs

In Figure D3, the feedback capacitor is too large. Settling is smooth, although overdamped, and a 600ns penalty results. Figure D4's feedback capacitor is too small, causing a somewhat underdamped response with resultant excessive ring time excursions. Settling time goes out to 2.3µs.

When feedback capacitors are individually trimmed for optimal response, the DAC, amplifier and compensation capacitor tolerances are irrelevant. If individual trimming is not used, these tolerances must be considered to determine the feedback capacitor's production value. Ring time is affected by DAC capacitance and resistance, as well as the feedback capacitor's value. The relationship is nonlinear, although some guidelines are possible. The DAC impedance terms can vary by ±50% and the feedback capacitor is typically a ±5% component. Additionally, amplifier slew rate has a significant tolerance, which is stated on the data sheet. To obtain a production feedback capacitor value, determine the optimum value by individual trimming *with the production board layout* (board layout parasitic capacitance counts too!). Then, factor in the worst-case percentage values for DAC impedance terms, slew rate and feedback capacitor tolerance. Add this information to the trimmed capacitors measured value to obtain the production value. This budgeting is perhaps unduly pessimistic (RMS error summing may be a defensible compromise), but will keep you out of trouble.[2] Figure 34's "conservative" settling time values were arrived at in this manner. Note that the chart's slow slewing amplifiers have the same compensation capacitor for "optimal" and "conservative" cases. This reflects the fact that their ring times are very small compared to their slew intervals.

Note 2: The potential problems with RMS error summing become clear when sitting in an airliner that is landing in a snowstorm.

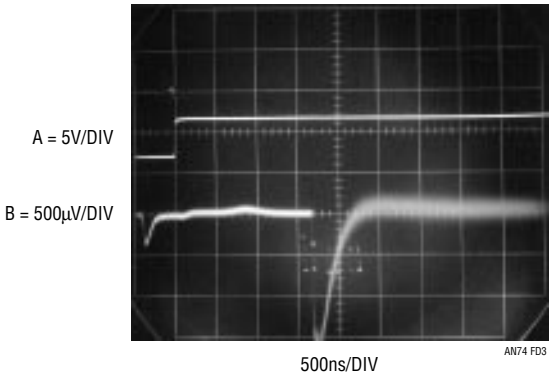

Figure D3. Overdamped Response Ensures Freedom from Ringing, Even with Component Variations in Production. Penalty is Increased Settling Time. t_{SETTLE} = 2.3µs

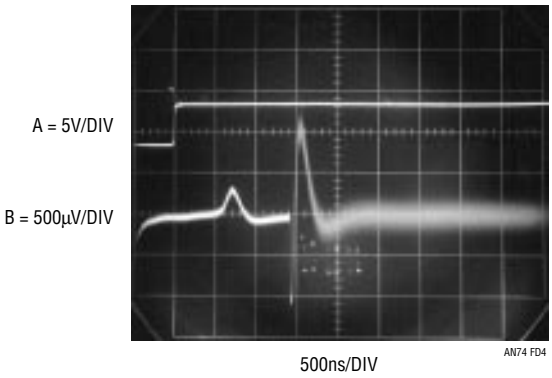

Figure D4. Underdamped Response Results from Undersized Capacitor. Component Tolerance Budgeting Will Prevent This Behavior. t_{SETTLE} = 2.3µs

APPENDIX E

A VERY SPECIAL CASE—MEASURING SETTLING TIME OF CHOPPER-STABILIZED AMPLIFIERS

Figure 34's table lists the LTC1150 chopper-stabilized amplifier. The term "special case" appears in the "comments" column. A special case it is! To see why requires some understanding of how these amplifiers work. Figure E1 is a simplified block diagram of the LTC1150 CMOS chopper-stabilized amplifier. There are actually two amplifiers. The "fast amp" processes input signals directly to the output. This amplifier is relatively quick, but has poor DC offset characteristics. A second, clocked, amplifier is employed to periodically sample the offset of the fast channel and maintain its output "hold" capacitor at whatever value is required to correct the fast amplifier's offset errors. The DC stabilizing amplifier is clocked to permit it to operate (internally) as an AC amplifier, eliminating its DC terms as an error source.[1] The clock chops the stabilizing amplifier at about 500Hz, providing updates to the hold capacitor-offset control every 2ms.[2]

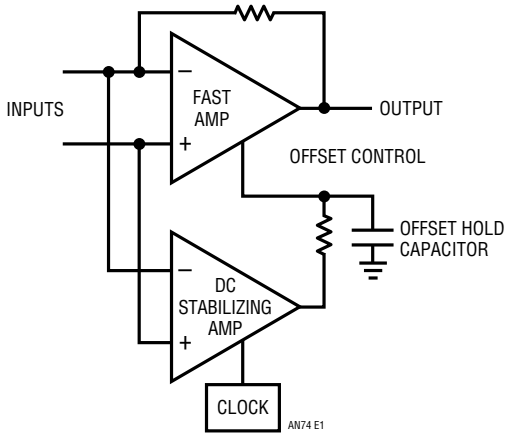

Figure E1. Highly Simplified Block Diagram of Monolithic Chopper-Stabilized Amplifier. Clocked Stabilizing Amplifier and Hold Capacitor Cause Settling Time Lag

The settling time of this composite amplifier is a function of the response of the fast and stabilizing paths. Figure E2 shows short-term settling of the amplifier. Trace A is the DAC input pulse and trace B the settle signal. Damping is reasonable and the 10µs settling time and profile appear typical. Figure E3 brings an unpleasant surprise. If the DAC slewing interval happens to coincide with the amplifier's sampling cycle, serious error is induced. In Figure E3, trace A is the amplifier output and trace B the settle signal. Note the slow horizontal scale. The amplifier initially settles quickly (settling is visible in the 2nd vertical division region) but generates a huge error 200µs later when its internal clock applies an offset correction. Successive clock cycles progressively chop the error into the noise but 7 *milliseconds* are required for complete recovery. The error derives from the fact that the amplifier sampled its

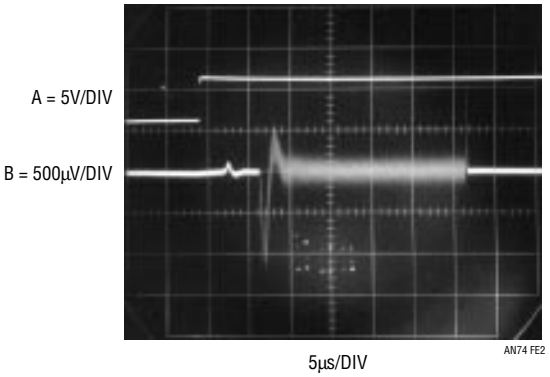

Figure E2. Short-Term Settling Profile of Chopper-Stabilized Amplifier Seems Typical. Settling Appears to Occur in 10µs

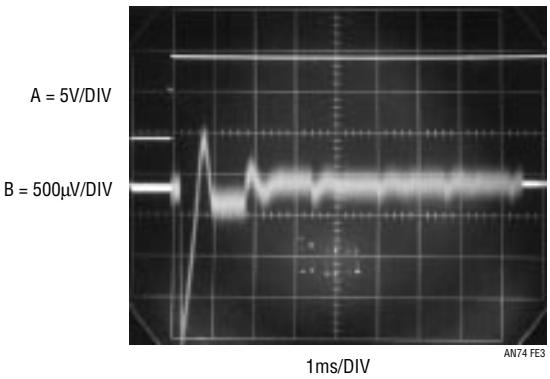

Figure E3. Surprise! Actual Settling Requires 700× More Time Than Figure E2 Indicates. Slow Sweep Reveals Monstrous Tailing Error (Note Horizontal Scale Change) Due to Amplifier's Clocked Operation. Stabilizing Loop's Iterative Corrections Progressively Reduce Error Before Finally Disappearing Into Noise

offset when its input was driven well outside its bandpass. This caused the stabilizing amplifier to acquire erroneous offset information. When this "correction" was applied, the result was a huge output error.

This is admittedly a worst case. It can only happen if the DAC slewing interval coincides with the amplifier's internal clock cycle, but it can happen.[3, 4]

Note 1: This AC processing of DC information is the basis of all chopper and chopper-stabilized amplifiers. In this case, if we could build an inherently stable CMOS amplifier for the stabilizing stage, no chopper stabilization would be necessary.

Note 2: Those finding this description intolerably brief are commended to reference 23.

Note 3: Readers are invited to speculate on the instrumentation requirements for obtaining Figure E3's photo.

Note 4: The spirit of Appendix D's footnote 2 is similarly applicable in this instance.

APPENDIX F

SETTLING TIME MEASUREMENT OF SERIALLY LOADED DACS

LTC models LTC1595 and LTC1650 are serially loaded 16-bit DACs. The LTC1650 includes an onboard output amplifier. Measuring these device's settling time with the methods described in the text requires additional circuitry. The circuitry must provide a "start" pulse to the settling time measurement after serially loading a full-scale step into the DAC. Figure F1's circuitry, designed and constructed by Jim Brubaker, Kevin Hoskins, Hassan Malik and Tuyet Pham (all of LTC) does this. The "start" pulse is taken from U1B's Q output. The DAC amplifier is monitored in the normal manner. This permits Figure F2 to display settling results in (what should be by now) familiar fashion. Settling time (trace B) is measured from the rising edge of trace A's start pulse. Figure F3 is a similar circuit configured for the LTC1650 voltage output DAC. Reference voltage and other changes are required to accommodate the DAC's ±4V output swing and different architecture, but overall operation is similar. Figure F4 shows settling results.

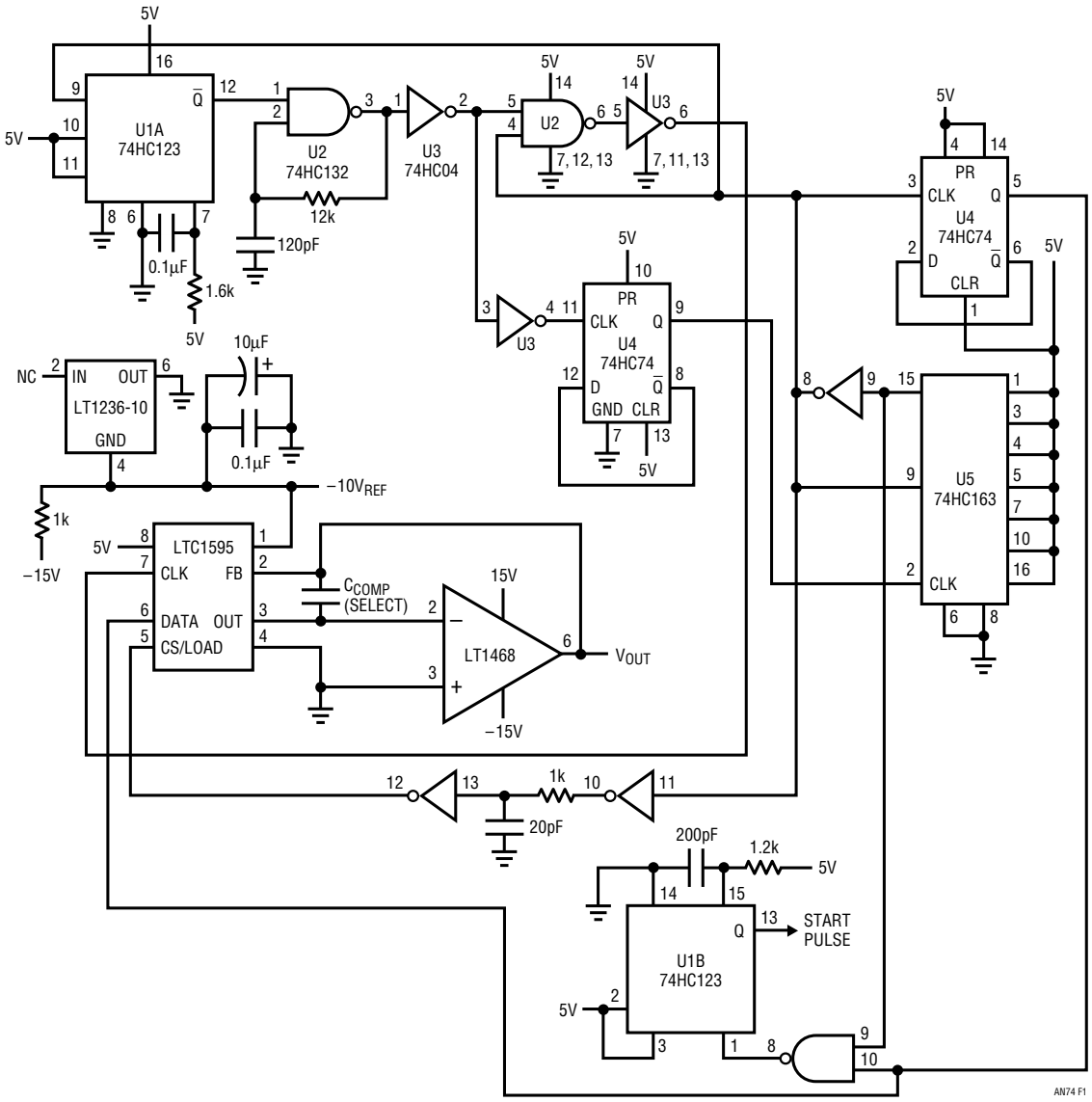

Figure F1. Logic Circuitry Permits Measuring Settling Time of Serially Loaded LTC1595 DAC

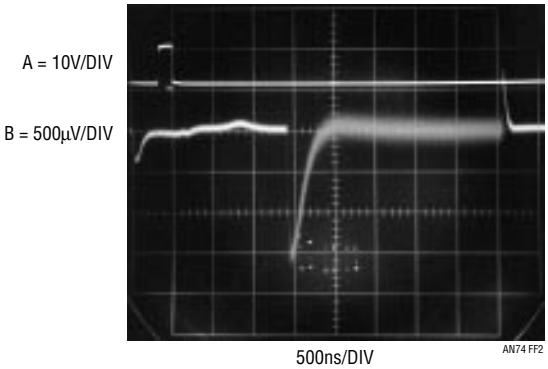

Figure F2. Oscilloscope Display of Serially Loaded DAC Settling Time Measurement. Settling Time is Measured from "Start Pulse" (See Schematic) Rising Edge (Trace A)

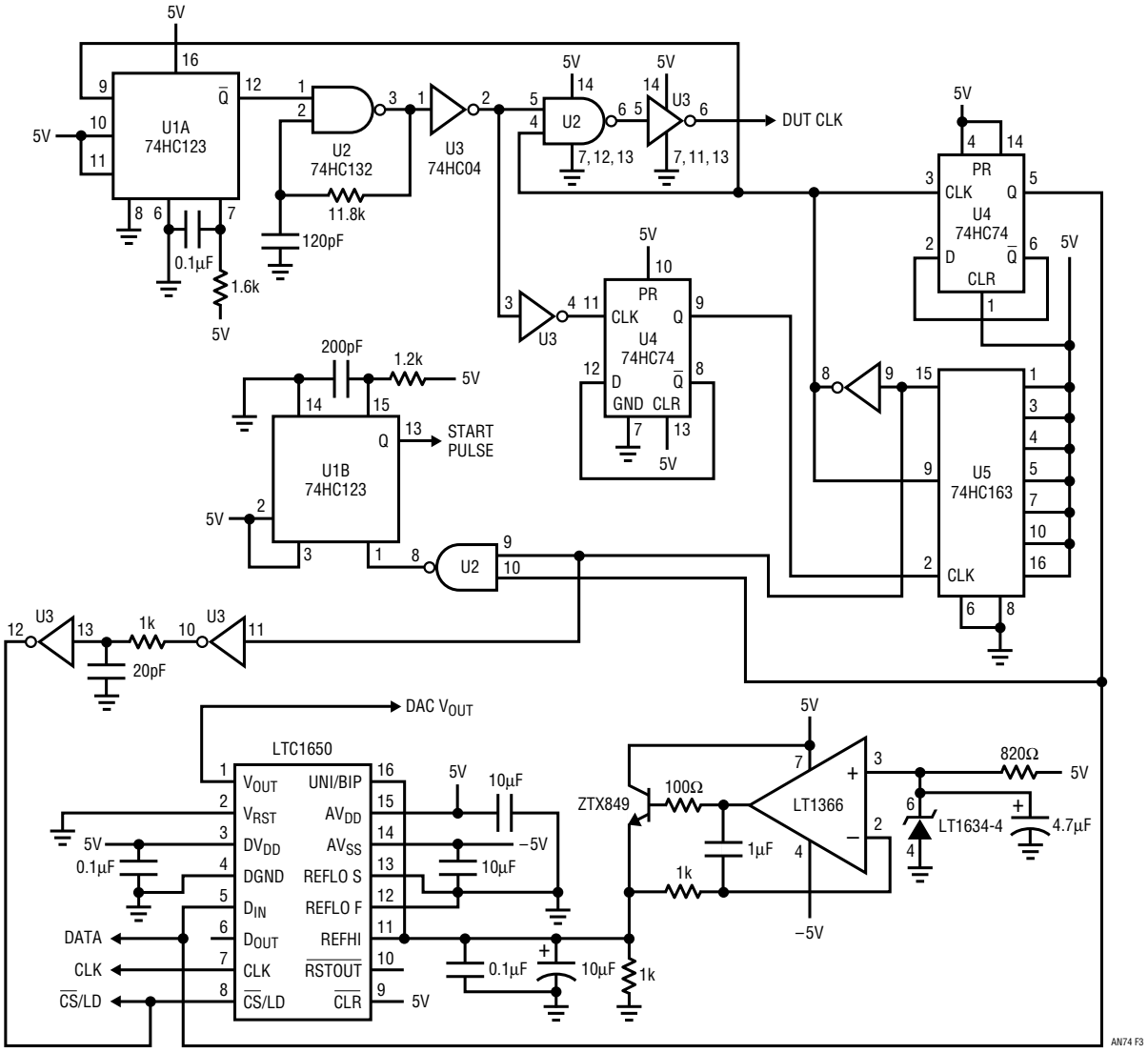

Figure F3. Reconfigured Figure F1 Allows LTC1650 Settling Time Measurement

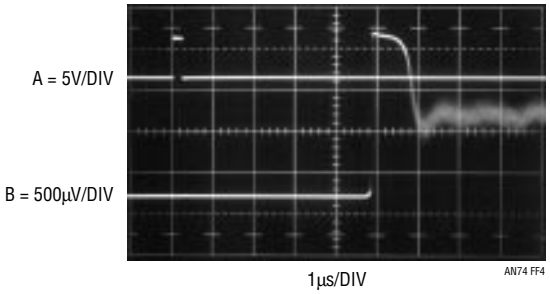

Figure F4. LTC1650 Voltage Output DAC Shows 6µs Settling Time. A is Start Pulse, B the Settle Signal

APPENDIX G

BREADBOARDING, LAYOUT AND CONNECTION TECHNIQUES

The measurement results presented in this publication required painstaking care in breadboarding, layout and connection techniques. Wideband, 100μV resolution measurement does not tolerate cavalier laboratory attitude. The oscilloscope photographs presented, devoid of ringing, hops, spikes and similar aberrations, are the result of an exhaustive (and frustrating) breadboarding exercise.[1] The sampler-based breadboard (Figures G1, G2) was rebuilt six times and required days of layout and shielding experimentation before obtaining a noise/uncertainty floor worthy of 16-bit measurement.

Ohm's Law

It is worth considering that Ohm's law is a key to successful layout.[2] Consider that 1mA running through 0.1Ω generates 100μV—almost 1LSB at 16 bits! Now, run that milliampere at 5 to 10 nanosecond rise times (≈75MHz) and the need for layout care becomes clear. A paramount concern is disposal of circuit ground return current and disposition of current in the ground plane. The impedance of the ground plane between any two points is *not* zero, particularly as frequency scales up. This is why the entry point and flow of "dirty" ground returns must be carefully placed within the grounding system. In the sampler-based breadboard, the approach was separate "dirty" and "signal" ground planes (see Figures G1 to G7), tied together at the supply ground origin.

A good example of the importance of grounding management involves delivering the input pulse to the breadboard. The pulse generator's 50Ω termination *must* be an in-line coaxial type, and it cannot be directly tied to the signal ground plane. The high speed, high density (5V pulses through the 50Ω termination generate 100mA current spikes) current flow must return directly to the pulse generator. The coaxial terminator's construction ensures this substantial current does this, instead of being dumped into the signal ground plane (100mA termination current flowing through 1 *milliohm* of ground plane produces ≈1LSB of error!). Figure G3 shows that the BNC shield floats from the signal plane, and is returned to "dirty" ground via RF braid. Additionally, Figure G1 shows the pulse generator's 50Ω termination physically distanced from the breadboard via a coaxial extension tube. This further ensures that pulse generator return current circulates in a tight local loop at the terminator, and does not mix into the signal plane.

It is worth mentioning that every ground return in the entire circuit must be evaluated with these concerns in mind. A paranoiac mindset is quite useful.

Shielding

The most obvious way to handle radiation-induced errors is shielding. Various following figures show shielding. Determining where shields are required should come *after* considering what layout will minimize their necessity. Often, grounding requirements conflict with minimizing radiation effects, precluding maintaining distance[3] between sensitive points. Shielding[4] is usually an effective compromise in such situations.

A similar approach to ground path integrity should be pursued with radiation management. Consider what points are likely to radiate, and try to lay them out at a distance from sensitive nodes. When in doubt about odd effects, experiment with shield placement and note results, iterating towards favorable performance.[5] *Above all, never rely on filtering or measurement bandwidth limiting to "get rid of" undesired signals whose origin is not fully understood.* This is not only intellectually dishonest, but may produce wholly invalid measurement "results," even if they look pretty on the oscilloscope.

Note 1: "War" is perhaps a more accurate descriptive.

Note 2: I do not wax pedantic here. My abuse of this postulate runs deep.

Note 3: Distance is the physicist's approach to reducing radiation induced effects.

Note 4: Shielding is the engineer's approach to reducing radiation induced effects.

Note 5: After it works, you can figure out why.

Connections

All signal connections to the breadboard must be coaxial. Ground wires used with oscilloscope probes are forbidden. A 1" ground lead used with a 'scope probe can easily generate several LSBs of observed "noise"! Use coaxially mounting probe tip adapters![6]

Figures G1 to G10 restate the above sermon in visual form while annotating the text's measurement circuits.

Note 6: See Reference 26 for additional nagging along these lines.

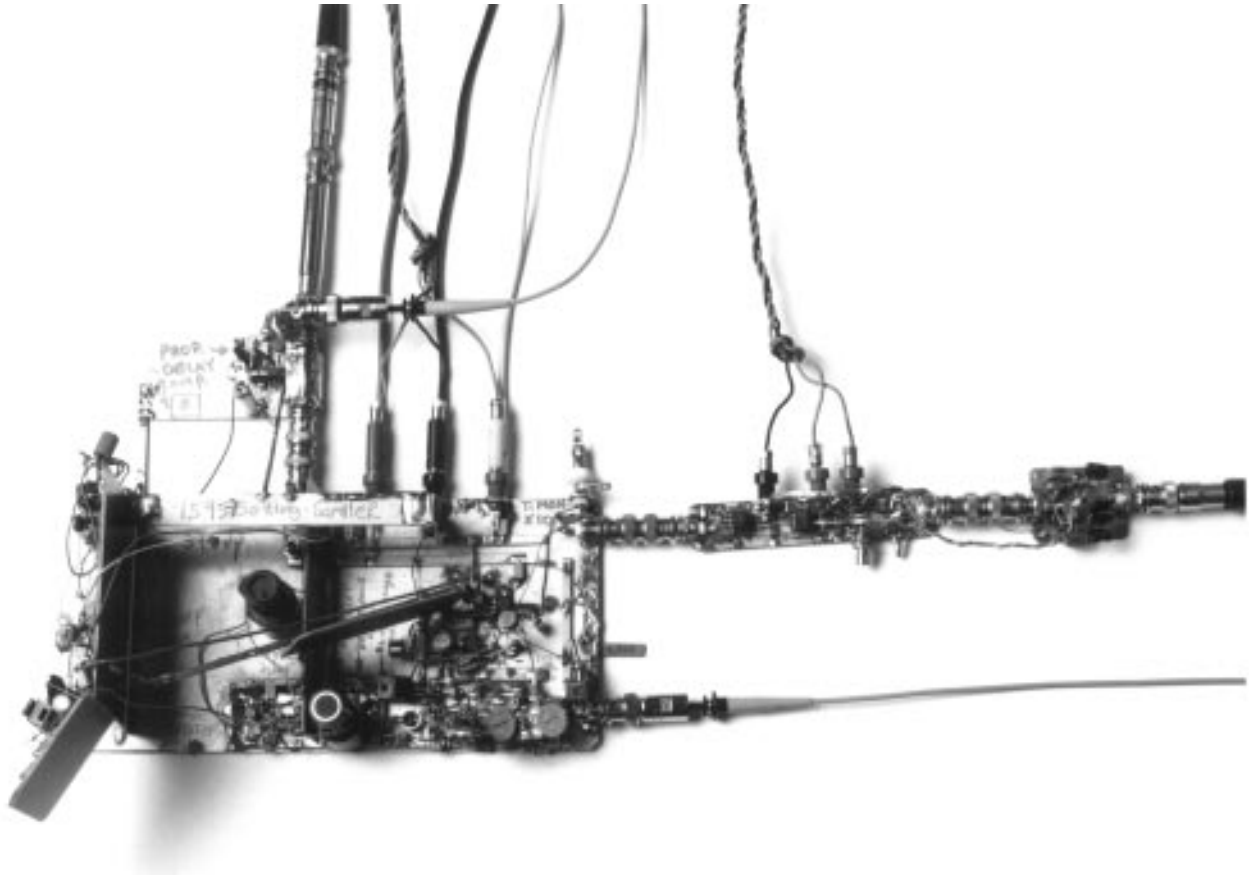

Figure G1. Overview of Settling Time Breadboard. Pulse Generator Input Enters Top Left—50Ω Coaxial Terminator Mounted On Extension Minimizes Pulse Generator Return Current Mixing Into Signal Ground Plane (Bottom Board Facing Viewer). "Dirty" Ground Paths Return Separately from Signal Ground Plane Via Planed Horizontal Strip (Upper Left of Main Board). DAC-Amplifier and Support Circuitry are at Extreme Left on Vertical Board. Sampler Circuitry Occupies Board Lower Center. Nonsaturating Amplifier-Bootstrapped Clamp is Thin Board, Extreme Right. Note Coaxial Board Signal and Probe Connections

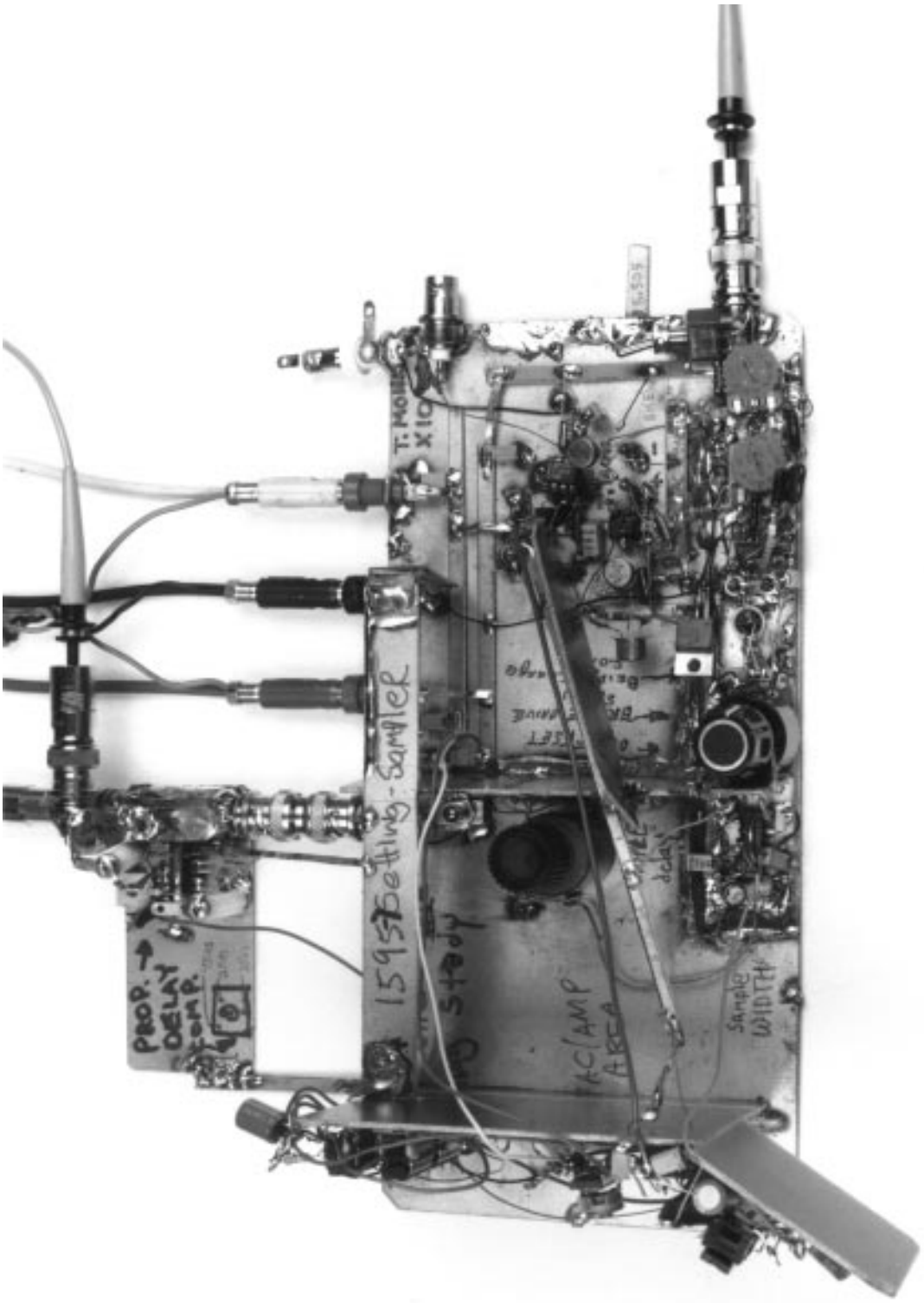

Figure G2. Settling Time Breadboard Detail. Note Radiation Shielding at Delayed Pulse Generator (Lower Left Center), Sampling Bridge Area (Lower Center Right) and DAC-Amplifier Board (Extreme Left). "Dirty" Grounds Return Via Separate Plane (Horizontal Strip, Photo Center Left). Vertical Shield (Center) Bisects Board, Separating Delayed Pulse Generator's (Lower Left Center) Fast Edges from Sampling Bridge Circuitry. DAC Amplifier Output is Routed Via Thin Copper Strip (Angled, Running Left-Right) to Settle Node (Board Center Right). Shield (Angled, Center) Prevents Radiation Into Bridge Area

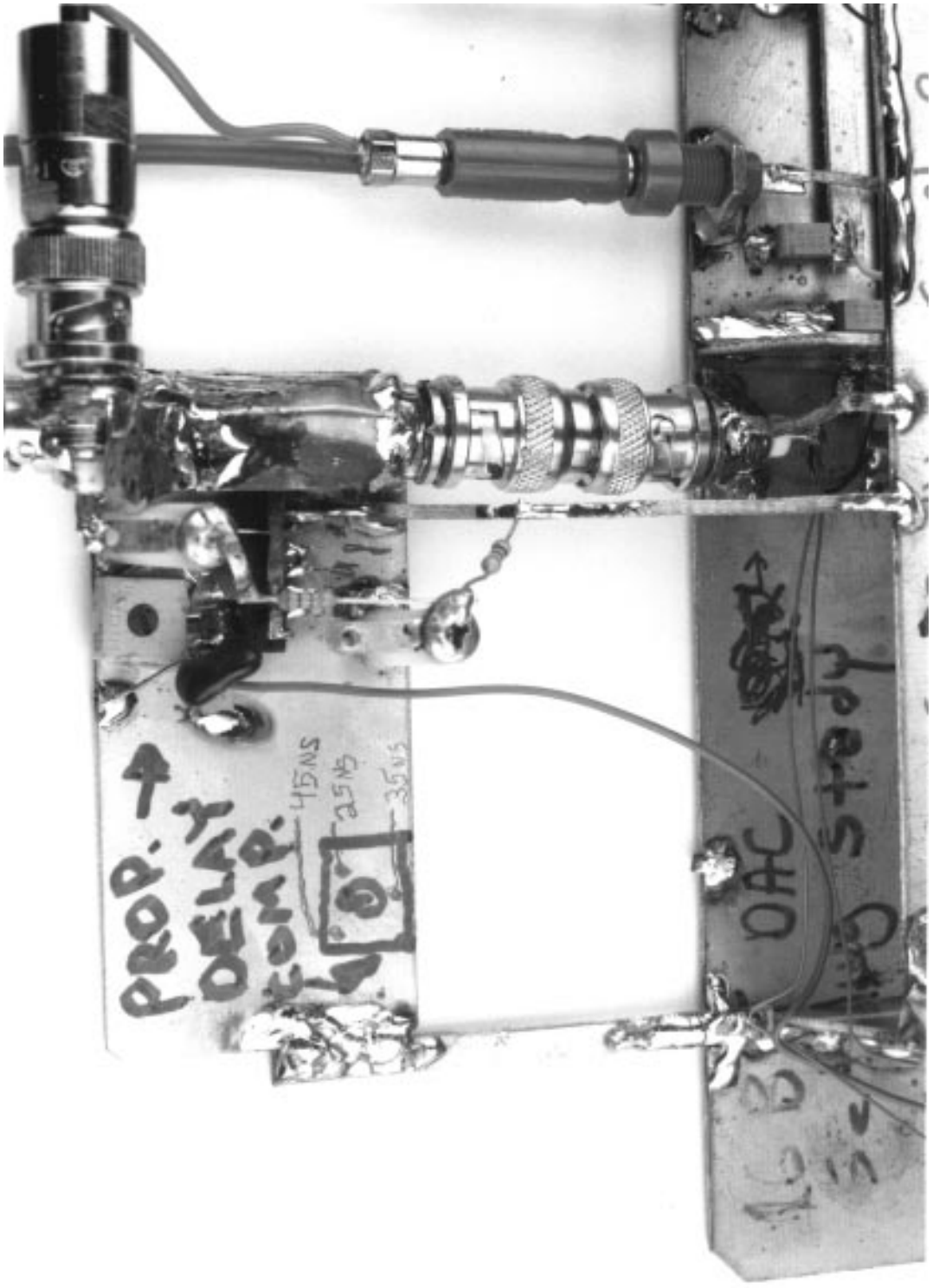

Figure G3. Detail of Pulse Generator Input—Delay Compensation Section and Interface to Main Board. Time Correction Delay Circuitry is at Photo Upper Center. Coaxial Probe Pick-Off Upper Right. Time Corrected Pulse Enters Main Board at Lower Center Plane (Clad Stand-Off Just Visible at Lower Connector Right). Connector Shell Ground is Tied To "Dirty" Ground Plane Via RF Braid (Lower Right Center), Preventing High Speed Return Currents from Corrupting Main Board Signal Ground Plane. Active Current Returns Flow Through Separate Braid (Long Vertical Run, Photo Center Right) to Main Board "Dirty" Ground Plane

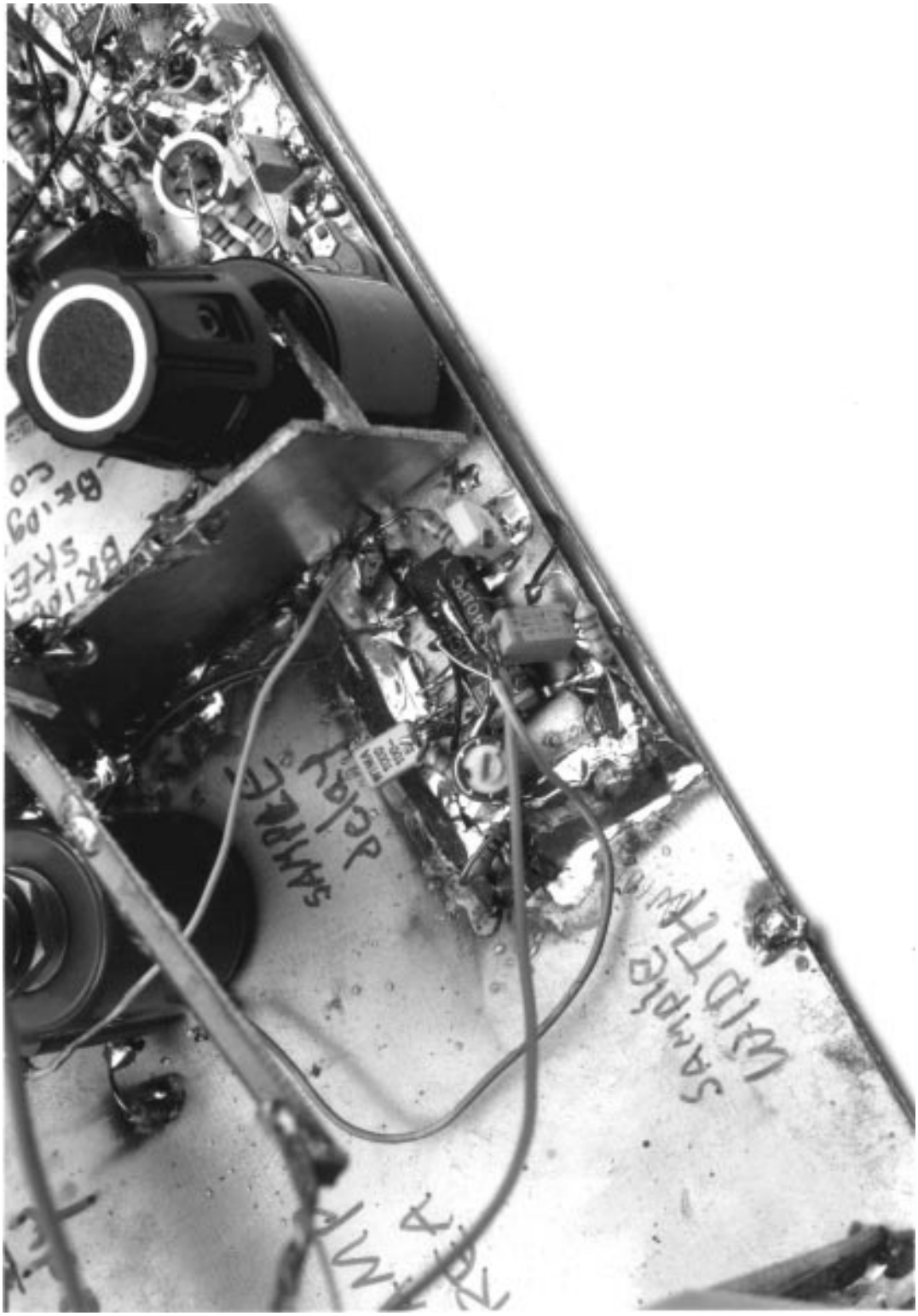

Figure G4. Delayed Pulse Generator is Fully Shielded (Vertical Shield, Photo Center Right) from Sampling Circuitry (Partial, to Right of Vertical Shield). Delayed Pulse Generators Output Lead (Photo Center) Sneaks Under Main Ground Plane to Minimize Radiation Into Sampling Bridge. Screw Adjustment (Photo Center Left) Sets Delayed Pulse Width, Large Potentiometer (Partial, Photo Upper Left Center) Sets Delay

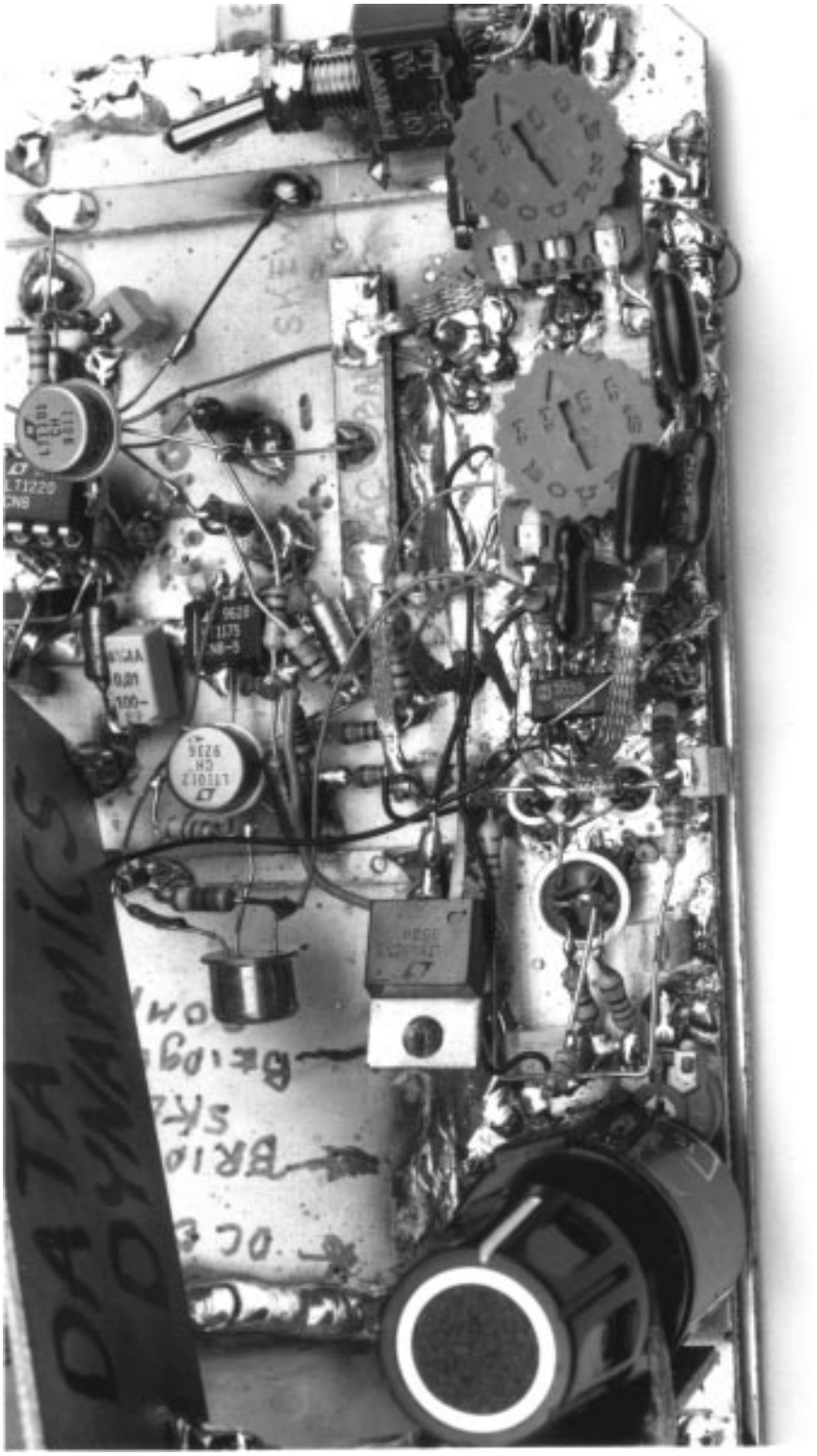

Figure G5. Sampling Bridge and Support Circuitry. Delayed Pulse Generator Output Arrives from Under Ground Plane (Photo Center, Just to Right of TO-220 Power Package), Triggers Complementary Level Shifters (Center Left). Sampling Bridge is SOT-16 Package at Photo Center. Skew Compensation and Bridge AC Balance Trimpots are at Photo Center Right. Baseline Zero is Large Knob at Left. Sampling Bridge Temperature Control Circuitry Appears Upper Right Center

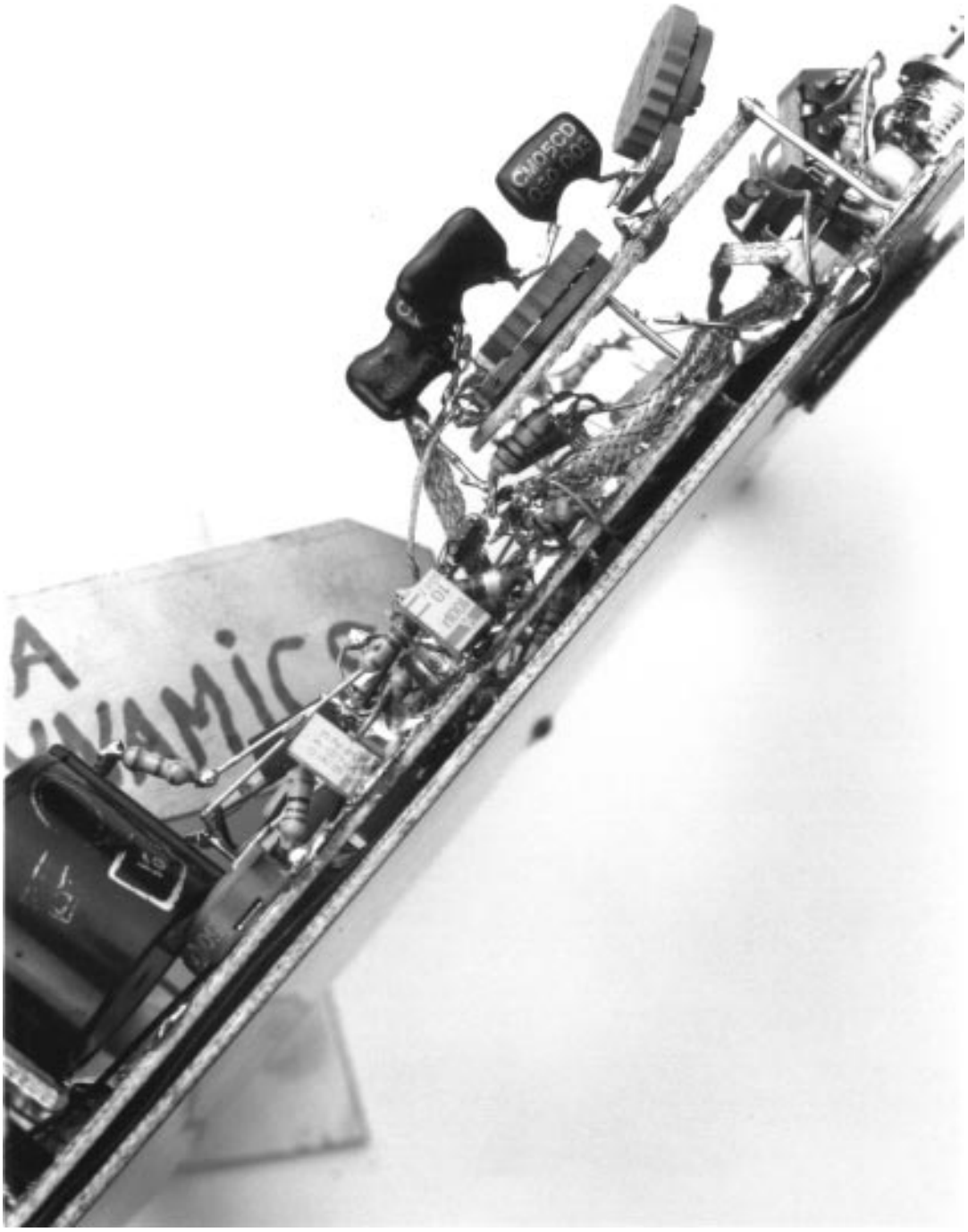

Figure G6. Side-On View of Sampling Bridge Circuitry. Delayed Pulse Generator Output Line is Just Visible in Shielded Space Under Ground Plane (≈45° Angle, Photo Extreme Left, Running Towards Center). SOT-16 Packaged Sampling Bridge (Exact Photo Center) Floats on Flying Leads to Maximize Thermal Resistance, Aiding Temperature Control. Upper Board (Photo Right) Mechanically Supports AC Bridge Trimpots

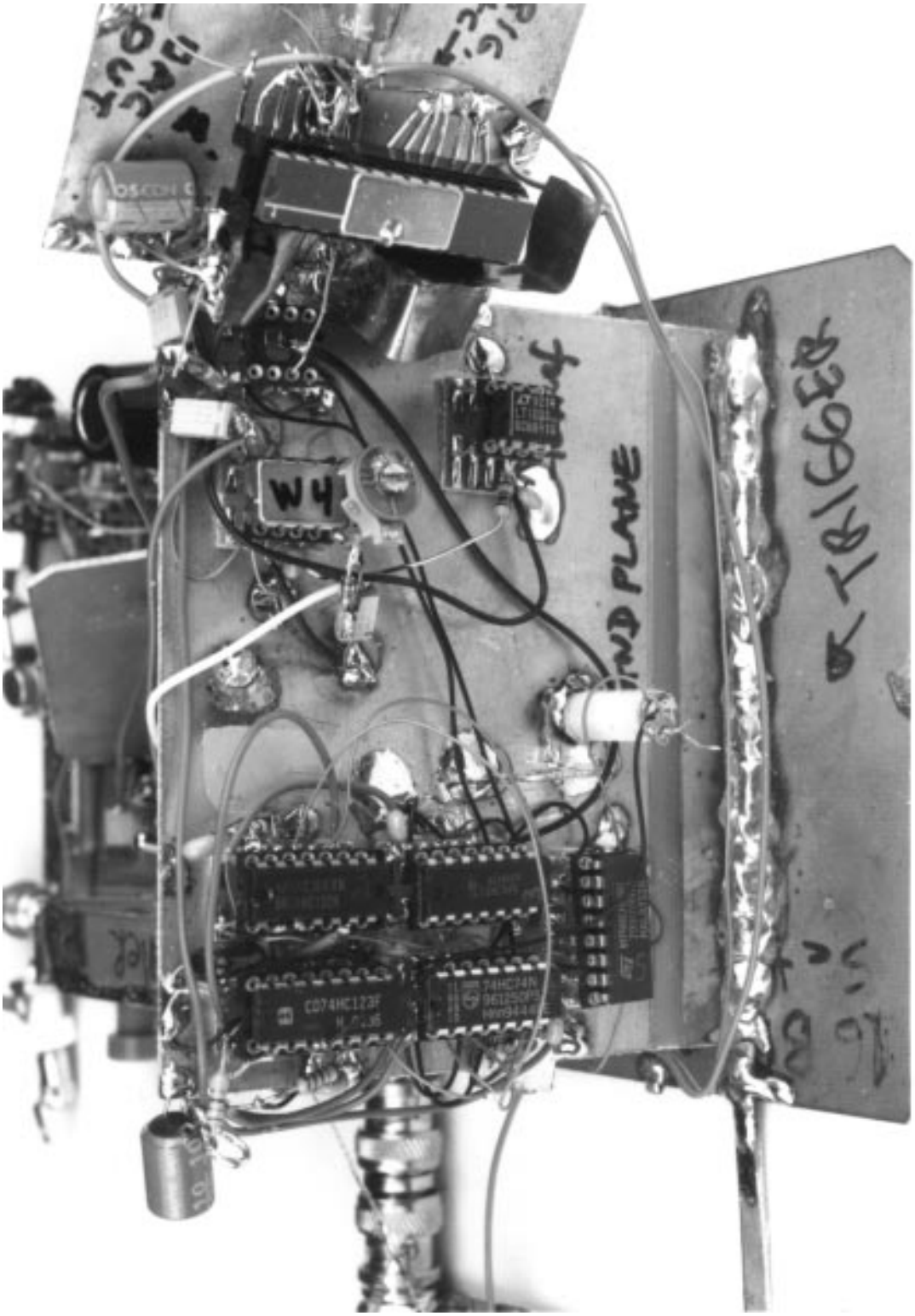

Figure G7. DAC-Amplifier Board Contains DAC (Right), Amplifier ("W4" at Center Right) and Reference (Lower Right). Digital IC Packages at Left are Serial DAC Interface, Potential Noise Generators. Insulating Strip Across Entire Board Bottom Fully Isolates it from Main Board Signal Ground Plane. Individual Board Returns are Routed Separately to Main Board Power Common

Figure G8. Gain-of-80 Nonsaturating Amplifier (Right of BNC Adapter) and Bootstrapped Clamp (Left of BNC Adapter). Ground Planed Construction and Minimized Summing Point Capacitances Aid Wideband Response

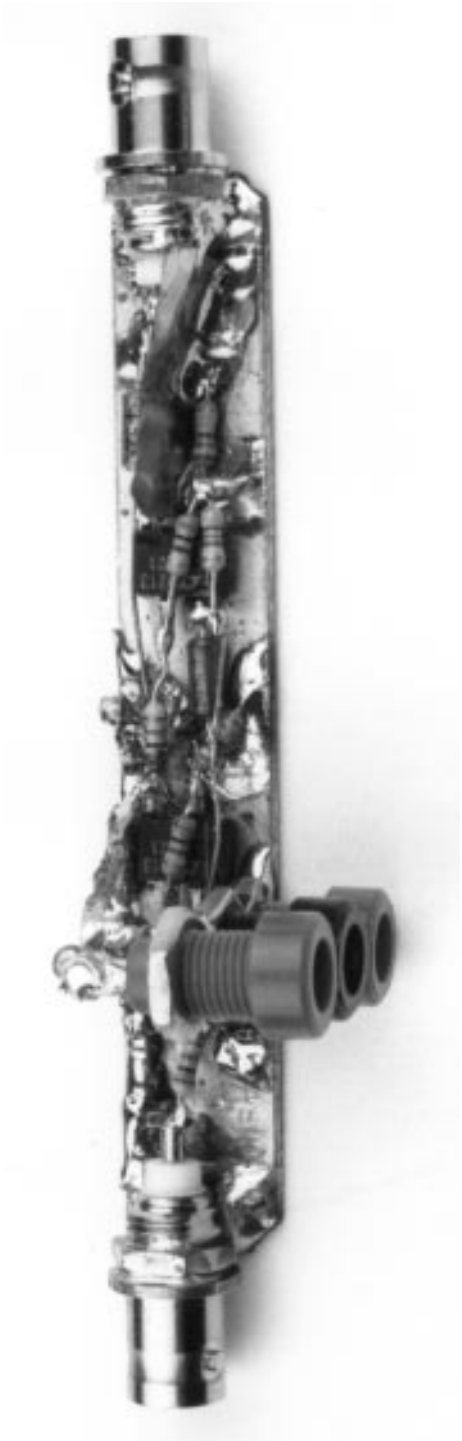

Figure G9. Wideband Nonsaturating Gain of 40 for Figure 28's Differential Amplifier. Layout Ensures Minimal Feedthrough, Particularly When Amplifier is Outside Gain Region. Note Input Shield (Photo Right)

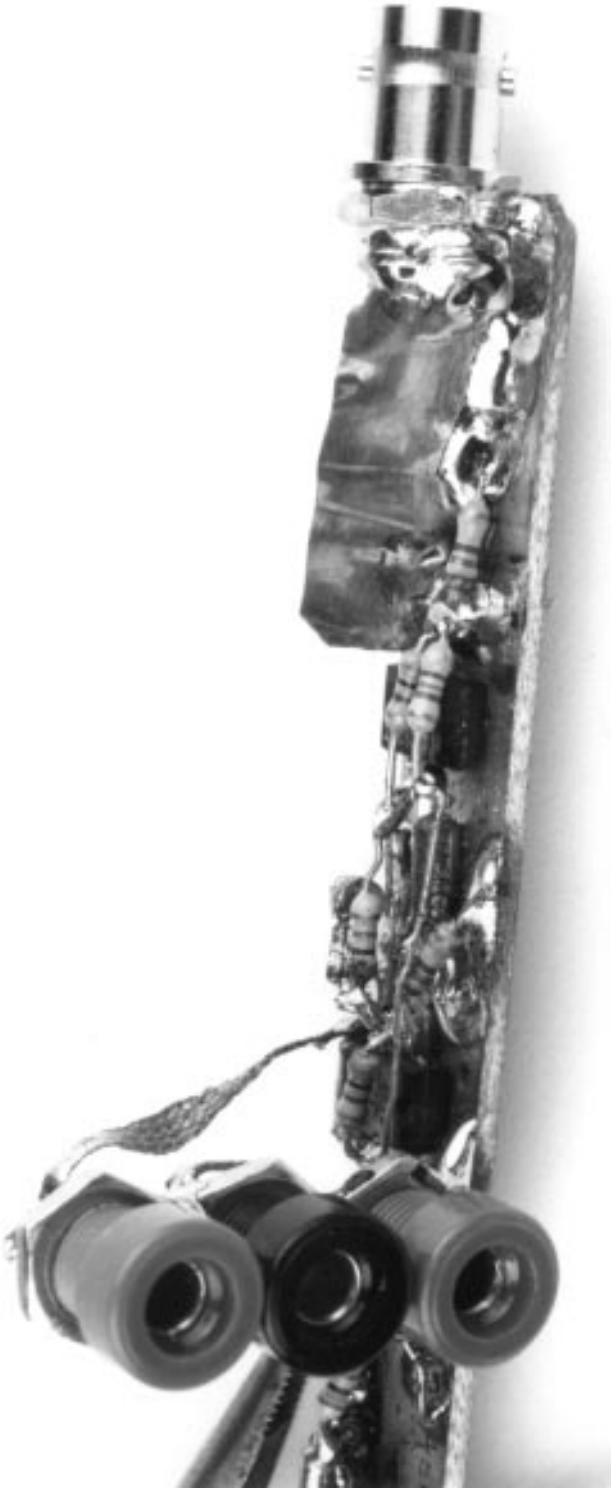

Figure G10. Detail of Nonsaturating Gain of 40 Input Shielding (Photo Right). Shield Prevents Input Excursions Outside Amplifier's Gain Region from Feeding Through to Output, Corrupting Data

APPENDIX H

POWER GAIN STAGES FOR HEAVY LOADS AND LINE DRIVING

Some applications require driving heavy loads. The load may be static, transient or both. Practical examples of loads include actuators, cables and power voltage/current sources in test equipment. Required load currents may range from tens of milliamperes to amperes, while simultaneously maintaining 16-bit performance. Figure H1 summarizes the system problems involved in applying a power gain stage, sometimes referred to as a booster.

The booster stage's output impedance must be low enough to accurately drive complex loads at all frequencies of interest. "Complex" loads may include interconnecting cable capacitance, pure resistance, capacitive and inductive components. Significant effort should be expended to characterize the load prior to designing the booster. Note that reactive load components will almost certainly add a stability term, complicating wideband loop dynamics. These considerations dictate that the booster's output impedance must be exceptionally low at all frequencies encountered.

Also, the booster must be fast to avoid delay-induced stability problems. Any booster included in an amplifier's loop must be transparent to the amplifier to preserve dynamic performance.[1]

Grounding and connection considerations mandate special attention in a high current, 16-bit, DAC driven system. A 1A load current returning through 1mΩ of parasitic resistance causes almost 7LSBs of error. Similar errors occur if feedback sensing is improperly arranged. As such, single-point grounding, in the strictest sense of the word, is mandatory. In particular, the load-return conductor should be thick, short, flat and highly conductive. Feedback sensing should be arranged so that the DAC's R_{FB} terminal is connected *directly* to the load via a low impedance conductor.

Note 1: This discussion must suffer brevity in this forum. For more detail, see References 26 and 27.

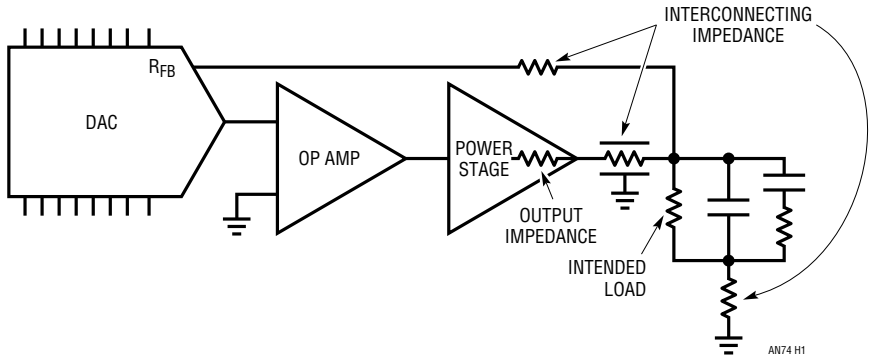

Figure H1. Conceptual Power Gain Stage for DAC-Amplifier. System Issues Involve Booster Output Impedance, Interconnections, Load Characteristics and Grounding

Booster Circuits

Figure H2 is a simple power output stage using the LT1010 IC booster. Output currents to 125mA are practical. Figure H3 is similar, although offering higher speed operation and more output power. The LT1206 op amp, configured as a unity-gain follower, permits 250mA outputs; the LT1210 extends current capacity to 1.1A. The indicated optional capacitor improves dynamic performance with capacitive loading (see data sheets). Figure H4 extends current output capacity to 2A by utilizing a wideband

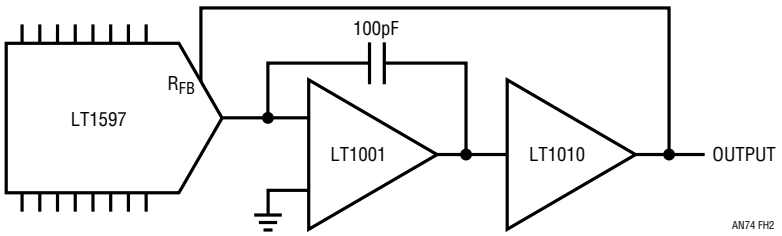

Figure H2. LT1010 Permits 125mA Output Currents

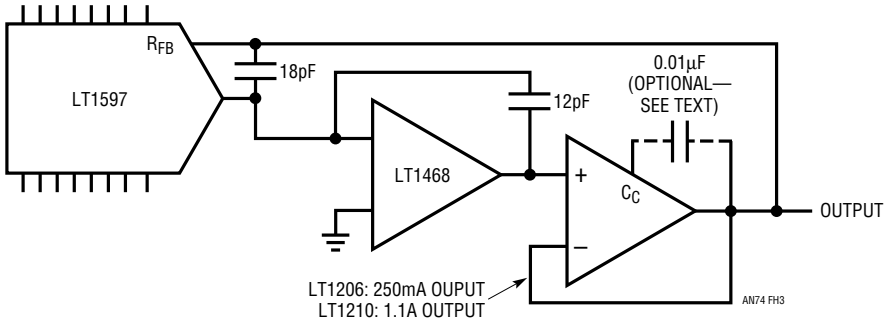

Figure H3. LT1206/LT1210 Output Stages Supply 250mA and 1.1A Loads, Respectively

discrete state. In the positive signal-path output transistor Q4 is an RF power type, driven by Darlington connected Q3. The diode in Q1's emitter compensates the additional V_{BE} introduced by Q3, preventing crossover distortion.

The negative signal path substitutes the Q5-Q6 connection to simulate a fast PNP power transistor. This arrangement is necessitated by the lack of availability of wideband PNP power transistors. Although this configuration acts like a fast PNP follower, it has voltage gain and tends to oscillate. The local 2pF feedback capacitor suppresses these parasitic oscillations and the composite transistor is stable.

This circuit also includes a feedback capacitor to optimize AC response. Current limiting is provided by Q7 and Q8, which sense across the 0.2Ω shunts.

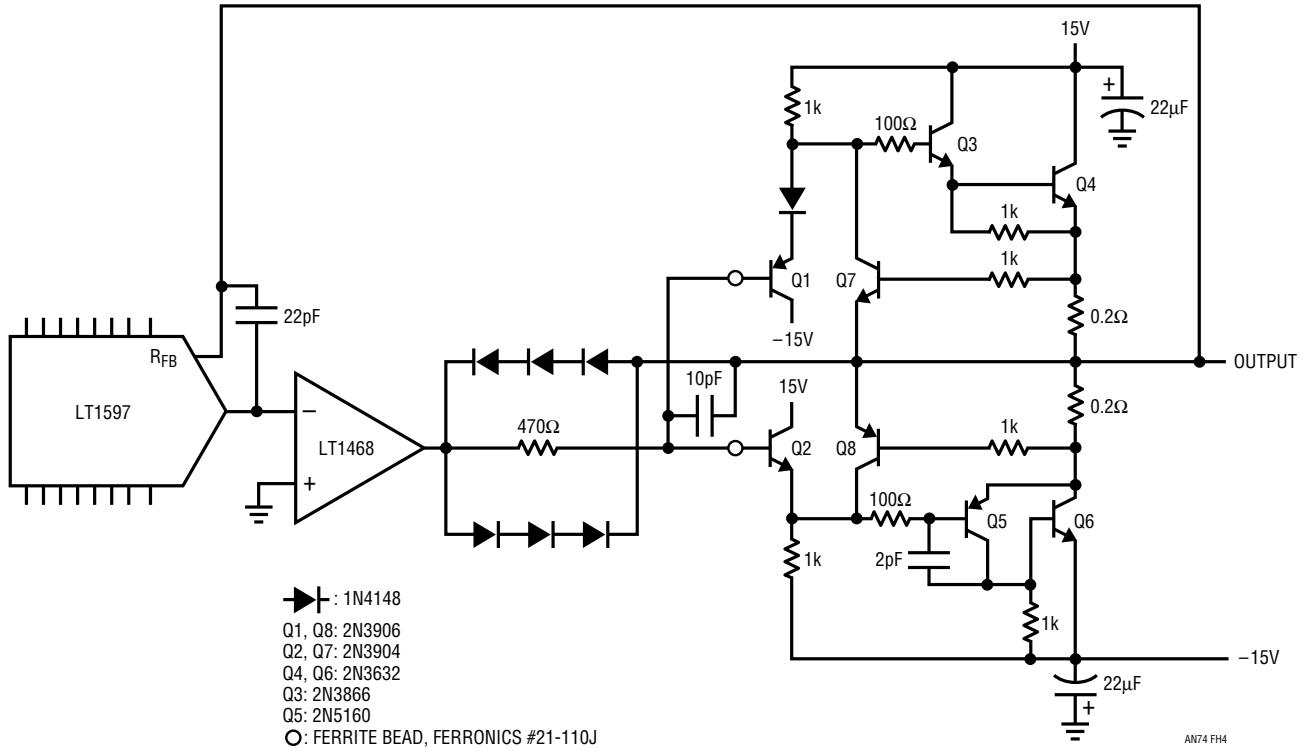

Figure H4. Wideband Discrete Component Booster is More Complex, But Supplies 2A Output

Figure H5 is a voltage gain stage. The high voltage stage is driven in closed-loop fashion by A2, instead of being included in the DAC-amplifier (A1) loop. This avoids driving the DAC's monolithic feedback resistor from the 100V output, preserving DAC temperature coefficient and, not incidentally, the DAC. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing ±12V A2 drives to cause full ±120V output swing. The local feedback reduces stage gain-bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low f_ts, and no special high frequency roll-off precautions are needed. Because the stage inverts, feedback is returned to A2's positive input. Frequency compensation is achieved by rolling off A2 with the local 330pF-10k pair. The 15pF capacitor in the feedback peaks edge response and is not required for stability. If over compensation is required, it is preferable to increase the 330pF value, instead of increasing the 15pF loop-feedback capacitor. This prevents excessive high voltage energy from coupling to A2's inputs during slew. If it is necessary to increase the feedback capacitor, the summing point should be diode clamped to ground or to the ±15V supply terminals. Trimming involves selecting the indicated resistor for exactly 100.000V output with the DAC at full scale.

The dynamic response issues discussed in the text apply to all the above circuits.

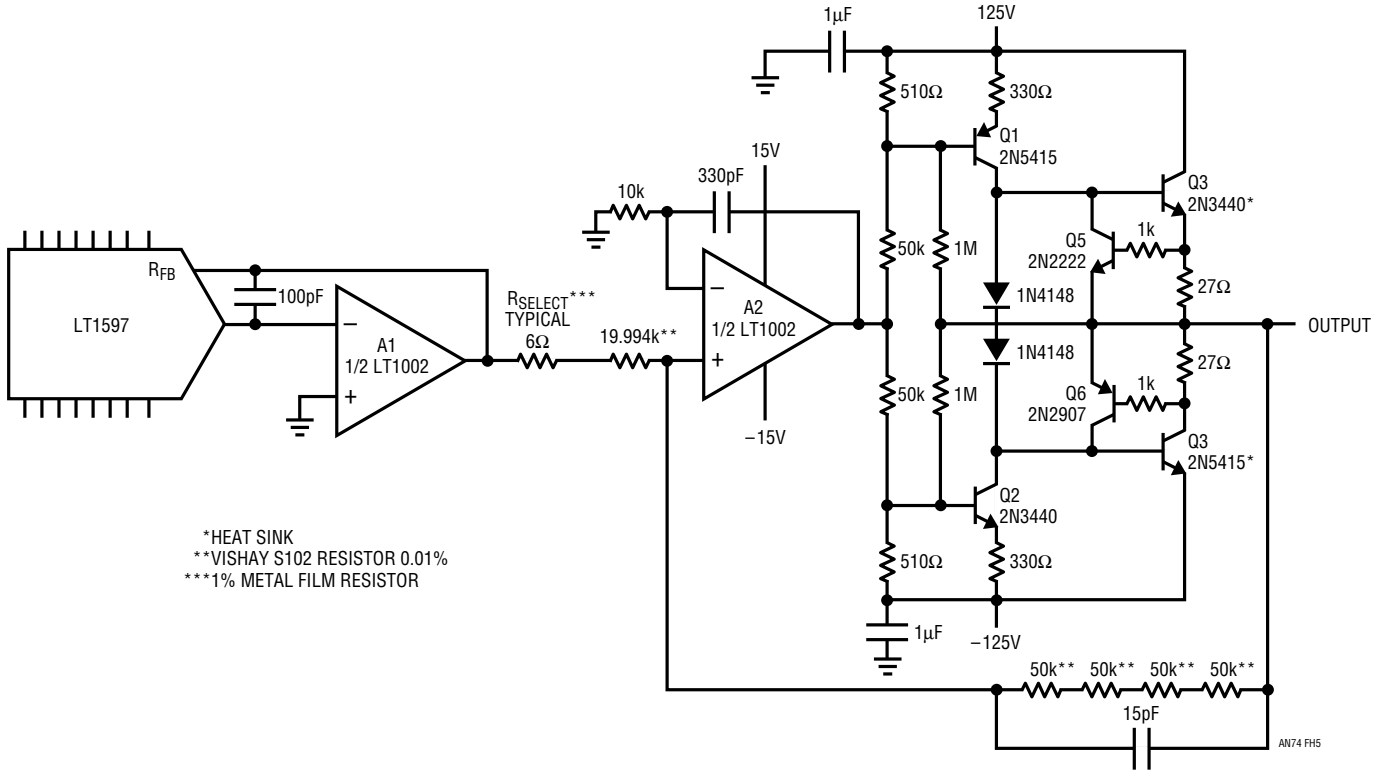

Figure H5. High Voltage Output Stage Delivers 100V at 25mA. Stage Uses Separate Amplifier and Feedback Resistors to Preserve DAC's Gain Temperature Coefficient

Figure H6 summarizes the booster stage's characteristics. The IC-based stages offer simplicity while the complex discrete designs provide more output power.

FIGURE	VOLTAGE GAIN	CURRENT GAIN	COMMENTS
H2	No	Yes	Simple 125mA Stage
H3	No	Yes	Simple 250mA/1.1A Stage
H4	No	Yes	Complex 2A Output
H5	Yes	Minimal	Complex ±120V Output

Figure H6. Summary of Booster Stage Characteristics

Measuring 16 Bit Settling Time is NOT A 1 week Project.

— WMW -98

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